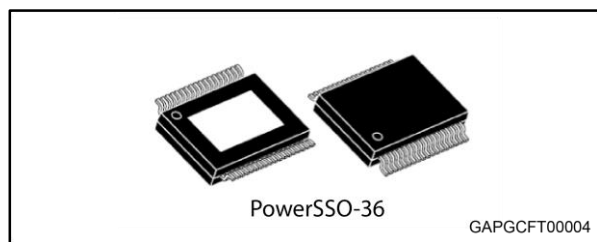


Quad channel high-side driver with MultiSense analog feedback for automotive applications

Datasheet - production data



- Load current limitation
- Self limiting of fast thermal transients
- Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
- Loss of ground and loss of V_{CC}
- Reverse battery through self turn-on
- Electrostatic discharge protection

Features

| | | |
|-----------------------------------|------------|---------------|
| Max transient supply voltage | V_{CC} | 41 V |
| Operating voltage range | V_{CC} | 4 to 28 V |
| Typ. on-state resistance (per ch) | R_{ON} | 40 m Ω |
| Current limitation (typ) | I_{LIMH} | 34 A |
| Standby current (max) | I_{STBY} | 0.5 μ A |

Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Turn Indicators (up to P27W or SAE1156 and R5W paralleled or LED Rear Combinations)

Description

The device is a quad channel high-side driver manufactured using the latest ST proprietary VIPower® technology and housed in a PowerSSO-36 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, and to provide protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions such as high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

The device features a dedicated LED Mode.

- AEC-Q100 qualified
- General
 - Quad channel smart high-side driver with MultiSense analog feedback
 - LED Mode for channel 0 and 1
 - Very low standby current
 - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
 - Multiplexed analog feedback of:
 - Load current with high precision proportional current mirror;
 - V_{CC} supply voltage;
 - T_{CHIP} device temperature
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
 - OFF-state open load detection
 - Output short to V_{CC} detection
 - Sense enable/disable
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp

Contents

| | | |
|----------|--|-----------|
| 1 | Block diagram and pin description | 6 |
| 2 | Electrical specification..... | 8 |
| 2.1 | Absolute maximum ratings | 8 |
| 2.2 | Thermal data | 9 |
| 2.3 | Electrical characteristics..... | 9 |
| 2.3.1 | General electrical specification..... | 9 |
| 2.3.2 | Bulb mode (default) | 17 |
| 2.3.3 | Electrical characteristics curves - Bulb Mode..... | 22 |
| 2.3.4 | LED Mode (Channel 0 and 1)..... | 25 |
| 2.3.5 | Electrical characteristics curves - LED mode..... | 28 |
| 2.3.6 | Truth tables..... | 30 |
| 3 | Protections..... | 32 |
| 3.1 | Power limitation..... | 32 |
| 3.2 | Thermal shutdown..... | 32 |
| 3.3 | Current limitation | 32 |
| 3.4 | Negative voltage clamp..... | 32 |
| 4 | Application information | 33 |
| 4.1 | GND protection network against reverse battery..... | 33 |
| 4.2 | Immunity against transient electrical disturbances | 34 |
| 4.3 | MCU I/Os protection..... | 34 |
| 4.4 | Multisense - analog current sense | 35 |
| 4.4.1 | Principle of Multisense signal generation..... | 36 |
| 4.4.2 | TCASE and VCC monitor | 38 |
| 4.4.3 | Short to VCC and OFF-state open-load detection | 39 |
| 5 | Maximum demagnetization energy (VCC = 16 V) | 40 |
| 6 | Package and PCB thermal data..... | 41 |
| 6.1 | PowerSSO-36 thermal data | 41 |
| 7 | Package information | 45 |
| 7.1 | PowerSSO-36 package information | 45 |
| 7.2 | PowerSSO-36 packing information | 47 |
| 7.3 | PowerSSO-36 marking information..... | 49 |
| 8 | Order codes | 50 |
| 9 | Revision history | 51 |

List of tables

| | |
|--|----|
| Table 1: Pin functions | 6 |
| Table 2: Suggested connections for unused and not connected pins | 7 |
| Table 3: Absolute maximum ratings | 8 |
| Table 4: Thermal data | 9 |
| Table 5: Power section | 9 |
| Table 6: Logic Inputs | 10 |
| Table 7: Protections | 12 |
| Table 8: MultiSense | 12 |
| Table 9: Power section in Bulb Mode | 17 |
| Table 10: Switching in Bulb Mode | 18 |
| Table 11: MultiSense in Bulb Mode | 19 |
| Table 12: Switching in LED Mode | 25 |
| Table 13: Power section in LED Mode | 25 |
| Table 14: MultiSense in LED Mode | 26 |
| Table 15: Truth table | 30 |
| Table 16: MultiSense multiplexer addressing | 30 |
| Table 17: Bulb/LED Mode Configuration | 31 |
| Table 18: ISO 7637-2 - electrical transient conduction along supply line | 34 |
| Table 19: MultiSense pin levels in off-state | 38 |
| Table 20: PCB properties | 42 |
| Table 21: Thermal parameters | 43 |
| Table 22: PowerSSO-36 mechanical data | 45 |
| Table 23: Reel dimensions | 47 |
| Table 24: PowerSSO-36 carrier tape dimensions | 48 |
| Table 25: Device summary | 50 |
| Table 26: Document revision history | 51 |

List of figures

| | |
|---|----|
| Figure 1: Block diagram | 6 |
| Figure 2: Configuration diagram (top view)..... | 7 |
| Figure 3: Current and voltage conventions..... | 8 |
| Figure 4: Switching times and Pulse skew | 16 |
| Figure 5: MultiSense timings (current sense mode) | 16 |
| Figure 6: Multisense timings (chip temperature and VCC sense mode) | 17 |
| Figure 7: TDSKON..... | 17 |
| Figure 8: Bulb Mode - IOUT/ISENSE versus IOUT | 21 |
| Figure 9: Bulb Mode - current sense precision vs. IOUT..... | 21 |
| Figure 10: OFF-state output current | 22 |
| Figure 11: Standby current | 22 |
| Figure 12: IGND(ON) vs. Iout | 22 |
| Figure 13: Logic Input high level voltage | 22 |
| Figure 14: Logic Input low level voltage..... | 22 |
| Figure 15: High level logic input current | 22 |
| Figure 16: Low level logic input current | 23 |
| Figure 17: Logic Input hysteresis voltage | 23 |
| Figure 18: FaultRST Input clamp voltage | 23 |
| Figure 19: Undervoltage shutdown..... | 23 |
| Figure 20: On-state resistance vs. Tcase | 23 |
| Figure 21: On-state resistance vs. VCC | 23 |
| Figure 22: Turn-on voltage slope | 24 |
| Figure 23: Turn-off voltage slope..... | 24 |
| Figure 24: Won vs. Tcase..... | 24 |
| Figure 25: Woff vs. Tcase..... | 24 |
| Figure 26: ILIMH vs. Tcase..... | 24 |
| Figure 27: OFF-state open-load voltage detection threshold | 24 |
| Figure 28: Vsense clamp vs. Tcase..... | 25 |
| Figure 29: Vsenseh vs. Tcase | 25 |
| Figure 30: LED Mode - IOUT/ISENSE versus IOUT | 27 |
| Figure 31: LED Mode - current sense precision vs. IOUT..... | 28 |
| Figure 32: On-state resistance vs. Tcase | 28 |
| Figure 33: On-state resistance vs. VCC | 28 |
| Figure 34: Turn-on voltage slope | 29 |
| Figure 35: Turn-off voltage slope..... | 29 |
| Figure 36: Won vs. Tcase..... | 29 |
| Figure 37: Woff vs. Tcase..... | 29 |
| Figure 38: ILIMH vs. Tcase..... | 29 |
| Figure 39: Application diagram | 33 |
| Figure 40: Simplified internal structure | 33 |
| Figure 41: MultiSense and diagnostic – block diagram | 35 |
| Figure 42: MultiSense block diagram | 36 |
| Figure 43: Analogue HSD – open-load detection in off-state | 37 |
| Figure 44: Open-load / short to VCC condition..... | 38 |
| Figure 45: GND voltage shift | 39 |
| Figure 46: Maximum turn off current versus inductance | 40 |
| Figure 47: PowerSSO-36 PC board | 41 |
| Figure 48: Rthj-amb vs PCB copper area in open box free air condition | 42 |
| Figure 49: PowerSSO-36 thermal impedance junction ambient..... | 43 |
| Figure 50: Thermal fitting model of a HSD in PowerSSO-36 | 43 |
| Figure 51: PowerSSO-36 package outline | 45 |
| Figure 52: PowerSSO-36 reel 13" | 47 |
| Figure 53: PowerSSO-36 carrier tape | 48 |

Figure 54: PowerSSO-36 schematic drawing of leader and trailer tape49
Figure 55: PowerSSO-36 marking information49

1 Block diagram and pin description

Figure 1: Block diagram

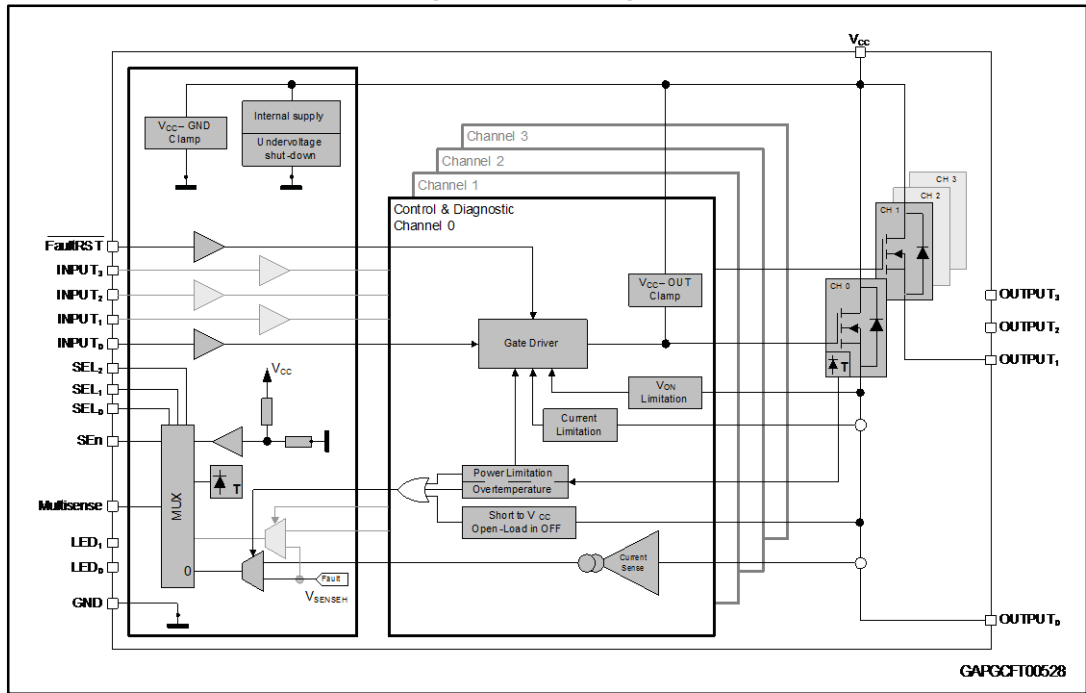


Table 1: Pin functions

| Name | Function |
|---------------------------|--|
| V _{CC} | Battery connection. |
| OUTPUT _{0,1,2,3} | Power output. |
| GND | Ground connection. |
| INPUT _{0,1,2,3} | Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. They control output switch state. |
| MultiSense | Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature. |
| SEn | Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin |
| LED _{0,1} | Active high compatible with 3 V and 5 V CMOS outputs pin; they enable the LED mode on logic high level (see Table 15: "Truth table"). |
| SEL _{0,1,2} | Active high compatible with 3 V and 5 V CMOS outputs pin; they address the MultiSense multiplexer (see Table 15: "Truth table"). |
| FaultRST | Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode. |

Figure 2: Configuration diagram (top view)

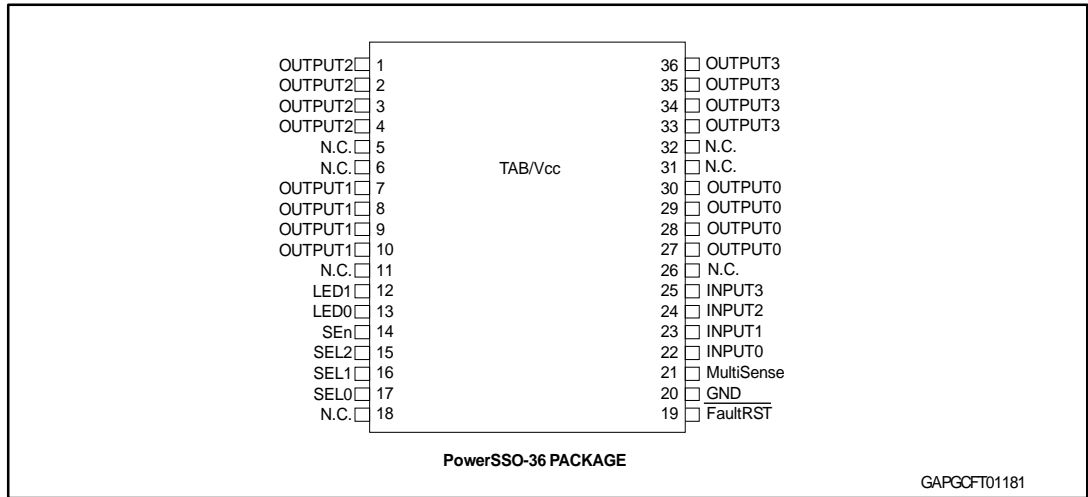


Table 2: Suggested connections for unused and not connected pins

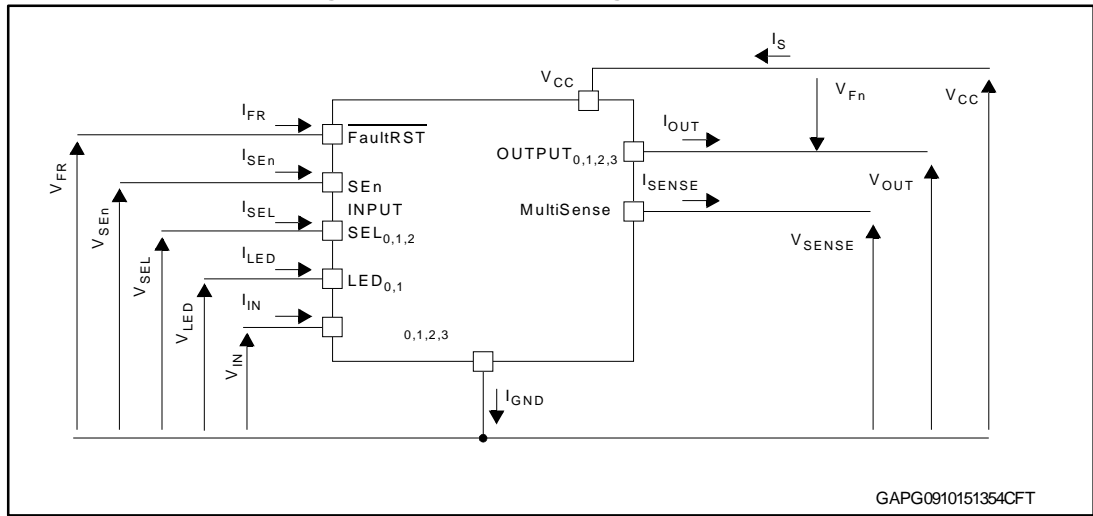
| Connection / pin | MultiSense | N.C. | Output | Input | SEn, SELx, LEDx, FaultRST |
|------------------|-----------------------|------------------|-------------|------------------------|---------------------------|
| Floating | Not allowed | X ⁽¹⁾ | X | X | X |
| To ground | Through 1 kΩ resistor | X | Not allowed | Through 15 kΩ resistor | Through 15 kΩ resistor |

Notes:

⁽¹⁾X: do not care.

2 Electrical specification

Figure 3: Current and voltage conventions



$$V_{FN} = V_{OUTn} - V_{CC}$$

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3: "Absolute maximum ratings"](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the table below for extended periods may affect device reliability.

Table 3: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------------------|---|--------------------|------|
| V _{CC} | DC supply voltage | 38 | V |
| -V _{CC} | Reverse DC supply voltage | 16 | |
| V _{CCPK} | Maximum transient supply voltage (ISO7637-2:2004 Pulse 5b level IV clamped to 40 V; R _L = 4 Ω) | 40 | |
| V _{CCJS} | Maximum jump start voltage for single pulse short circuit protection | 28 | |
| -I _{GND} | DC reverse ground pin current | 200 | mA |
| I _{OUT} | OUTPUT _{0,1,2,3} DC output current | Internally limited | A |
| -I _{OUT_0,1} | OUTPUT _{0,1} Reverse DC output current | 10 | |
| -I _{OUT_2,3} | OUTPUT _{2,3} Reverse DC output current | 10 | |
| I _{IN} | INPUT _{0,1,2,3} DC input current | -1 to 10 | mA |
| I _{LED} | LED _{0,1} DC input current | | |
| I _{SEn} | SEn DC input current | | |
| I _{SEL} | SEL _{0,1,2} DC input current | | |

| Symbol | Parameter | Value | Unit |
|--------------------|---|------------|------|
| I _{FR} | FaultRST DC input current | -1 to 10 | mA |
| V _{FR} | FaultRST DC input voltage | 7.5 | V |
| I _{SENSE} | MultiSense pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V) | -10 | mA |
| | MultiSense pin DC output current in reverse ($V_{CC} < 0$ V) | 20 | mA |
| E _{MAX} | Maximum switching energy (single pulse) ($T_{DEMAG} = 0.4$ ms; $T_{jstart} = 150$ °C) | 36 | mJ |
| V _{ESD} | Electrostatic discharge (JEDEC 22A-114F) | | |
| | • INPUT _{0,1,2,3} | 4000 | V |
| | • MultiSense | 2000 | V |
| | • LED _{0,1} , SEn, SEL _{0,1,2} , $\overline{\text{FaultRST}}$ | 4000 | V |
| | • OUTPUT _{0,1,2,3} | 4000 | V |
| | • V _{CC} | 4000 | V |
| V _{ESD} | Charge device model (CDM-AEC-Q100-011) | 750 | V |
| T _j | Junction operating temperature | -40 to 150 | °C |
| T _{stg} | Storage temperature | -55 to 150 | |

2.2 Thermal data

Table 4: Thermal data

| Symbol | Parameter | Typ. value | Unit |
|------------------------|---|------------|------|
| R _{thj-board} | Thermal resistance junction-board (JEDEC JESD 51-8) ⁽¹⁾⁽²⁾ | 4.9 | °C/W |
| R _{thj-amb} | Thermal resistance junction-ambient (JEDEC JESD 51-2) ⁽¹⁾⁽³⁾ | 53 | |
| R _{thj-amb} | Thermal resistance junction-ambient (JEDEC JESD 51-2) ⁽¹⁾⁽²⁾ | 18.5 | |

Notes:

⁽¹⁾One channel ON.

⁽²⁾Device mounted on four-layers 2s2p PCB

⁽³⁾Device mounted on two-layers 2s0p PCB with 2 cm² heatsink copper trace

2.3 Electrical characteristics

7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

2.3.1 General electrical specification

Table 5: Power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|-----------------------------|-----------------|------|------|------|------|
| V _{CC} | Operating supply voltage | | 4 | 13 | 28 | V |
| V _{USD} | Undervoltage shutdown | | | | 4 | |
| V _{USDReset} | Undervoltage shutdown reset | | | | 5 | |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|---|---|------|------|------|---------------|
| $V_{USDhyst}$ | Undervoltage shutdown hysteresis | | | 0.3 | | |
| V_{clamp} | Clamp voltage | $I_S = 20 \text{ mA}; 25 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ | 41 | 46 | 52 | V |
| | | $I_S = 20 \text{ mA}; T_j = -40 \text{ }^\circ\text{C}$ | 38 | | | V |
| I_{STBY} | Supply current in standby at $V_{CC} = 13 \text{ V}$ ⁽¹⁾ | $V_{CC} = 13 \text{ V};$ $V_{INx} = V_{OUTx} = V_{FR} = V_{SEn} = 0 \text{ V};$ $V_{SELO,1,2} = 0 \text{ V}; V_{LEDO,1} = 0 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C}$ | | | 0.5 | μA |
| | | $V_{CC} = 13 \text{ V};$ $V_{INx} = V_{OUTx} = V_{FR} = V_{SEn} = 0 \text{ V};$ $V_{SELO,1,2} = 0 \text{ V}; V_{LEDO,1} = 0 \text{ V};$ $T_j = 85 \text{ }^\circ\text{C}$ ⁽²⁾ | | | 0.5 | μA |
| | | $V_{CC} = 13 \text{ V};$ $V_{INx} = V_{OUTx} = V_{FR} = V_{SEn} = 0 \text{ V};$ $V_{SELO,1,2} = 0 \text{ V}; V_{LEDO,1} = 0 \text{ V};$ $T_j = 125 \text{ }^\circ\text{C}$ | | | 3 | μA |
| t_{D_STBY} | Standby mode blanking time | $V_{CC} = 13 \text{ V}; V_{INx} = V_{OUTx} = V_{FR} = 0 \text{ V};$ $V_{SELO,1,2} = 0 \text{ V}; V_{LEDO,1} = 0 \text{ V};$ $V_{SEn} = 5 \text{ V to } 0 \text{ V}$ | 60 | 300 | 550 | μs |
| $I_{S(ON)}$ | Supply current | $V_{CC} = 13 \text{ V};$ $V_{SEn} = V_{FR} = V_{SELO,1} = 0 \text{ V}; V_{INx} = 5 \text{ V};$ $I_{OUT0,1,2,3} = 0 \text{ A}$ | | 10 | 16 | mA |
| $I_{GND(ON)}$ | Control stage current consumption in ON state. All channels active. | $V_{CC} = 13 \text{ V}; V_{SEn} = 5 \text{ V};$ $V_{FR} = V_{SELO,1} = 0 \text{ V}; V_{INx} = 5 \text{ V};$ $I_{OUT0,1,2,3} = 2.5 \text{ A}$ | | | 18.5 | mA |
| $I_{L(off)}$ | Off-state output current at $V_{CC} = 13 \text{ V}$ ⁽¹⁾ | $V_{INx} = V_{OUTx} = 0 \text{ V}; V_{CC} = 13 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C}$ | 0 | 0.01 | 0.5 | μA |
| | | $V_{INx} = V_{OUTx} = 0 \text{ V}; V_{CC} = 13 \text{ V};$ $T_j = 125 \text{ }^\circ\text{C}$ | 0 | | 3 | |
| V_F | Output - V_{CC} diode voltage ⁽³⁾ | $I_{OUT} = -2.5 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$ | | | 0.7 | V |

Notes:

- (1)PowerMOS leakage included.
(2)Parameter specified by design; not subject to production test.
(3)For each channel.

Table 6: Logic Inputs

| 7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C | | | | | | |
|--|--------------------------|--------------------------|------|------|------|---------------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| INPUT_{0,1,2,3} characteristics | | | | | | |
| V_{IL} | Input low level voltage | | | | 0.9 | V |
| I_{IL} | Low level input current | $V_{IN} = 0.9 \text{ V}$ | 1 | | | μA |
| V_{IH} | Input high level voltage | | 2.1 | | | V |

| 7 V < V _{CC} < 28 V; -40 °C < T _j < 150 °C | | | | | | |
|--|--------------------------|-------------------------|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| I _{IH} | High level input current | V _{IN} = 2.1 V | | | 10 | μA |
| V _{I(hyst)} | Input hysteresis voltage | | 0.2 | | | V |
| V _{ICL} | Input clamp voltage | I _{IN} = 1 mA | 5.3 | | 7.2 | V |
| | | I _{IN} = -1 mA | | -0.7 | | |
| FaultRST characteristics | | | | | | |
| V _{FRL} | Input low level voltage | | | | 0.9 | V |
| I _{FRL} | Low level input current | V _{IN} = 0.9 V | 1 | | | μA |
| V _{FRH} | Input high level voltage | | 2.1 | | | V |
| I _{FRH} | High level input current | V _{IN} = 2.1 V | | | 10 | μA |
| V _{FR(hyst)} | Input hysteresis voltage | | 0.2 | | | V |
| V _{FRCL} | Input clamp voltage | I _{IN} = 1 mA | 5.3 | | 7.5 | V |
| | | I _{IN} = -1 mA | | -0.7 | | |
| SEL_{0,1,2} characteristics (7 V < V_{CC} < 18 V) | | | | | | |
| V _{SELL} | Input low level voltage | | | | 0.9 | V |
| I _{SELL} | Low level input current | V _{IN} = 0.9 V | 1 | | | μA |
| V _{SELH} | Input high level voltage | | 2.1 | | | V |
| I _{SELH} | High level input current | V _{IN} = 2.1 V | | | 10 | μA |
| V _{SEL(hyst)} | Input hysteresis voltage | | 0.2 | | | V |
| V _{SELCL} | Input clamp voltage | I _{IN} = 1 mA | 5.3 | | 7.2 | V |
| | | I _{IN} = -1 mA | | -0.7 | | |
| LED_{0,1} characteristics (7 V < V_{CC} < 18 V) | | | | | | |
| V _{LEDL} | Input low level voltage | | | | 0.9 | V |
| I _{LEDL} | Low level input current | V _{IN} = 0.9 V | 1 | | | μA |
| V _{LEDH} | Input high level voltage | | 2.1 | | | V |
| I _{LEDH} | High level input current | V _{IN} = 2.1 V | | | 10 | μA |
| V _{LED(hyst)} | Input hysteresis voltage | | 0.2 | | | V |
| V _{LEDCL} | Input clamp voltage | I _{IN} = 1 mA | 5.3 | | 7.2 | V |
| | | I _{IN} = -1 mA | | -0.7 | | |
| SEn characteristics (7 V < V_{CC} < 18 V) | | | | | | |
| V _{SEnL} | Input low level voltage | | | | 0.9 | V |
| I _{SEnL} | Low level input current | V _{IN} = 0.9 V | 1 | | | μA |
| V _{SEnH} | Input high level voltage | | 2.1 | | | V |
| I _{SEnH} | High level input current | V _{IN} = 2.1 V | | | 10 | μA |
| V _{SEn(hyst)} | Input hysteresis voltage | | 0.2 | | | V |
| V _{SEnCL} | Input clamp voltage | I _{IN} = 1 mA | 5.3 | | 7.2 | V |
| | | I _{IN} = -1 mA | | -0.7 | | |

Table 7: Protections

| 7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C | | | | | | |
|--|---|---|----------------------|----------------------|----------------------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| T _{TSD} | Shutdown temperature | | 150 | 175 | 200 | °C |
| T _R | Reset temperature ⁽¹⁾ | | T _{RS} + 1 | T _{RS} + 5 | | |
| T _{RS} | Thermal reset of fault diagnostic indication | V _{FR} = 0 V; V _{SEn} = 5 V | 135 | | | |
| T _{HYST} | Thermal hysteresis (T _{TSD} -T _R) ⁽¹⁾ | | | 5 | | |
| ΔT _{J_SD} | Dynamic temperature | | | 60 | | K |
| t _{LATCH_RST} | Fault reset time for output unlatch ⁽¹⁾ | V _{FR} = 5 V to 0 V; V _{SEn} = 5 V; V _{INx} = 5 V; V _{SEL0,1,2} = 0 V | 3 | 10 | 20 | μs |
| V _{DEMAG} | Turn-off output voltage clamp | I _{OUT} = 2 A; L = 6 mH; T _j = -40 °C | V _{CC} - 38 | | | V |
| | | I _{OUT} = 2 A; L = 6 mH; T _j = 25 °C to 150 °C | V _{CC} - 41 | V _{CC} - 46 | V _{CC} - 52 | V |
| V _{ON} | Output voltage drop limitation | I _{OUT} = 0.25 A | | 20 | | mV |

Notes:

⁽¹⁾Parameter guaranteed by design and characterization; not subject to production test.

Table 8: MultiSense

| 7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C | | | | | | |
|--|----------------------------|---|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| V _{SENSE_CL} | MultiSense clamp voltage | V _{SEn} = 0 V; I _{SENSE} = 1 mA | -17 | | -12 | V |
| | | V _{SEn} = 0 V; I _{SENSE} = -1 mA | | 7 | | V |
| Current Sense characteristics | | | | | | |
| I _{SENSE0} | MultiSense leakage current | MultiSense disabled: V _{SEn} = 0 V; | 0 | | 0.5 | μA |
| | | MultiSense disabled: ⁽¹⁾ -1 V < V _{SENSE} < 5 V | -0.5 | | 0.5 | |
| | | MultiSense enabled: V _{SEn} = 5 V All channels ON; I _{OUTX} = 0 A; Ch _x diagnostic selected; • E.g. Ch ₀ : V _{IN0} = 5 V; V _{IN1,2,3} = 5 V; V _{SEL0,1,2} = 0 V; I _{OUT0} = 0 A; I _{OUT1,2,3} = 2.5 A | 0 | | 2 | |

| 7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C | | | | | | |
|--|--|---|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| | | MultiSense enabled: V _{SEn} = 5 V Ch _x OFF; Ch _x diagnostic selected: <ul style="list-style-type: none"> E.g. Ch₀: V_{IN0} = 0 V; V_{IN1,2,3} = 5 V; V_{SELO,1,2} = 0 V; I_{OUT0} = 0 A; I_{OUT1,2,3} = 2.5 A | 0 | | 2 | |
| V _{OUT_MSD} ⁽¹⁾ | Output Voltage for MultiSense shutdown | V _{SEn} = 5 V; R _{SENSE} = 2.7 kΩ <ul style="list-style-type: none"> E.g. Ch₀: V_{IN0} = 5 V; V_{SELO,1,2} = 0 V; I_{OUT0} = 2.5 A | | 5 | | V |
| V _{SENSE_SAT} | Multisense saturation voltage | V _{CC} = 7 V; R _{SENSE} = 2.7 K; V _{SEn} = 5 V; V _{IN0} = 5 V; V _{SELO,1,2} = 0 V; I _{OUT0} = 4.5 A; T _j = 150°C | 5 | | | V |
| I _{SENSE_SAT} ⁽¹⁾ | CS saturation current | V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SELO,1,2} = 0 V; T _j = 150°C | 4 | | | mA |
| I _{OUT_SAT_BULB} ⁽¹⁾ | Output saturation current in BULB mode | V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SELO,1,2} = 0 V; T _j = 150°C | 8 | | | A |
| I _{OUT_SAT_LED} ⁽¹⁾ | Output saturation current in LED mode | V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SELO,1,2} = 0 V; T _j = 150°C | 2.3 | | | A |
| OFF-state diagnostic | | | | | | |
| V _{OL} | OFF state open load voltage detection threshold | V _{SEn} = 5V; Ch _x OFF; Ch _x diagnostic selected <ul style="list-style-type: none"> E.g. Ch₀: V_{IN0} = 0 V; V_{SELO,1,2} = 0 V | 2 | 3 | 4 | V |
| I _{L(off2)} | OFF state output sink current | V _{IN} = 0 V; V _{OUT} = V _{OL} ; T _j = -40°C to 125°C | -100 | | -15 | μA |
| t _{DSTKON} | OFF state diagnostic delay time from falling edge of INPUT (see Figure 4: "Switching times and Pulse skew") | V _{SEn} = 5 V; Ch _x ON to OFF transition; Ch _x diagnostic selected <ul style="list-style-type: none"> E.g. Ch₀: V_{IN0} = 5 V to 0 V; V_{SELO,1,2} = 0 V; V_{OUT0} > 4 V | 100 | 350 | 700 | μs |
| t _{D_OL_V} | Settling time for valid OFF-state open load diagnostic indication from rising edge of SE _n | V _{INx} = 0 V; V _{FR} = 0 V; V _{SELO,1,2} = 0 V; V _{OUT0} = 4 V; V _{SEn} = 0 V to 5 V | | | 60 | μs |

| 7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C | | | | | | |
|--|--|--|-------|------|-------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| t _{D_VOL} | OFF state diagnostic delay time from rising edge of V _{OUT} | V _{SEn} = 5V; Ch _X OFF; Ch _X diagnostic selected • E.g. Ch ₀ : V _{IN0} = 0 V; V _{SEL0,1,2} = 0 V; V _{OUT0} = 0 V to 4 V | | 5 | 30 | µs |
| Chip temperature analog feedback | | | | | | |
| V _{SENSE_TC} | MultiSense output voltage proportional to chip temperature | V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ; V _{INx} = 0 V; T _j = -40°C | 2.325 | 2.41 | 2.495 | V |
| | | V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ; V _{INx} = 0 V; T _j = 25°C | 1.985 | 2.07 | 2.155 | V |
| | | V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ; V _{INx} = 0 V; T _j = 125°C | 1.435 | 1.52 | 1.605 | V |
| dV _{SENSE_TC} /dT ⁽²⁾ | Temperature coefficient | T _j = -40°C to 150°C | | -5.5 | | mV/K |
| Transfer function | | V _{SENSE_TC} (T) = V _{SENSE_TC} (T ₀) + dV _{SENSE_TC} /dT * (T-T ₀) | | | | |
| V_{CC} supply voltage analog feedback | | | | | | |
| V _{SENSE_VCC} | MultiSense output voltage proportional to V _{CC} supply voltage | V _{CC} = 13 V; V _{SEn} = 5 V; V _{SEL0,1,2} = 5 V; V _{INx} = 0 V; R _{SENSE} = 1 kΩ | 3.16 | 3.23 | 3.3 | V |
| Transfer function ⁽²⁾ | | V _{SENSE_VCC} = V _{CC} / 4 | | | | |
| Fault diagnostic feedback (see Table 15: "Truth table") | | | | | | |
| V _{SENSEH} | MultiSense output voltage in fault condition | V _{CC} = 13 V; R _{SENSE} = 1 kΩ | 5 | | 6.6 | V |
| I _{SENSEH} | MultiSense output current in fault condition | V _{CC} = 13 V; V _{SENSE} = 5 V | 7 | 20 | 30 | mA |
| MultiSense timings (Chip Temperature Sense mode - see Figure 6: "Multisense timings (chip temperature and VCC sense mode)") | | | | | | |
| t _{DSSENSE3H} | V _{SENSE_TC} settling time from rising edge of SEn | V _{SEn} = 0 V to 5 V; V _{SEL0} = V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ | | | 60 | µs |
| t _{DSSENSE3L} | V _{SENSE_TC} disable delay time from falling edge of SEn | V _{SEn} = 5 V to 0 V; V _{SEL0} = V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ | | | 20 | µs |
| MultiSense timings (V_{CC} Voltage Sense mode - see Figure 6: "Multisense timings (chip temperature and VCC sense mode)") | | | | | | |

| 7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C | | | | | | |
|--|--|--|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| t _{DSSENSE4H} | V _{SENSE_VCC} settling time from rising edge of SEn | V _{SEn} = 0 V to 5 V; V _{SEL0} = V _{SEL1} = V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ | | | 60 | μs |
| t _{DSSENSE4L} | V _{SENSE_VCC} disable delay time from falling edge of SEn | V _{SEn} = 5 V to 0 V; V _{SEL0} = V _{SEL1} = V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ | | | 20 | μs |
| MultiSense Timings (Multiplexer transition times) ⁽³⁾ | | | | | | |
| t _{D_XtoY} | MultiSense transition delay from Ch _X to Ch _Y | V _{IN2} = 5 V; V _{IN3} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V to 5 V; V _{SEL1} = 5 V; V _{SEL2} = 0 V; I _{OUT2} = 0 A; I _{OUT3} = 2.5 A; R _{SENSE} = 1 kΩ | | | 20 | μs |
| t _{D_CStoTC} | MultiSense transition delay from current sense to T _C sense | V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = V _{SEL2} = 0 V to 5 V; I _{OUT0} = 1.25 A; R _{SENSE} = 1 kΩ | | | 60 | μs |
| t _{D_TCtoCS} | MultiSense transition delay from T _C sense to current sense | V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = V _{SEL2} = 5 V to 0 V; I _{OUT0} = 1.25 A; R _{SENSE} = 1 kΩ | | | 20 | μs |
| t _{D_CStoVCC} | MultiSense transition delay from current sense to V _{CC} sense | V _{IN2} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 5 V; V _{SEL1} = 5 V; V _{SEL2} = 0 V to 5 V; I _{OUT2} = 1.25 A; R _{SENSE} = 1 kΩ | | | 60 | μs |
| t _{D_VCCtoCS} | MultiSense transition delay from V _{CC} sense to current sense | V _{IN2} = 5 V; V _{SEn} = 5 V; V _{SEL1} = 5 V; V _{SEL0} = V _{SEL2} = 5 V to 0 V; I _{OUT2} = 1.25 A; R _{SENSE} = 1 kΩ | | | 20 | μs |
| t _{D_TCtoVCC} | MultiSense transition delay from T _C sense to V _{CC} sense | V _{SEn} = 5 V; V _{SEL1,2} = 5 V; V _{SEL0} = 0 V to 5 V; R _{SENSE} = 1 kΩ | | | 20 | μs |
| t _{D_VCCtoTC} | MultiSense transition delay from V _{CC} sense to T _C sense | V _{SEn} = 5 V; V _{SEL1,2} = 5 V; V _{SEL0} = 5 V to 0 V; R _{SENSE} = 1 kΩ | | | 20 | μs |
| t _{D_CStoVSENSEH} | MultiSense transition delay from stable current sense on Ch _X to V _{SENSEH} on Ch _Y | V _{IN0} = 5 V; V _{IN1} = 0 V; V _{OUT1} > 4 V; V _{SEn} = 5 V; V _{SEL2} = 0 V; V _{SEL1} = 0 V; V _{SEL0} = 0 V to 5 V; I _{OUT0} = 2.5 A; R _{SENSE} = 1 kΩ | | | 60 | μs |

Notes:

(1)Parameter guaranteed by design and characterization; not subject to production test.

⁽²⁾Vcc sensing and Tc sensing are referred to GND potential.

⁽³⁾Transition delay is measured up to +/- 10% of final conditions.

Figure 4: Switching times and Pulse skew

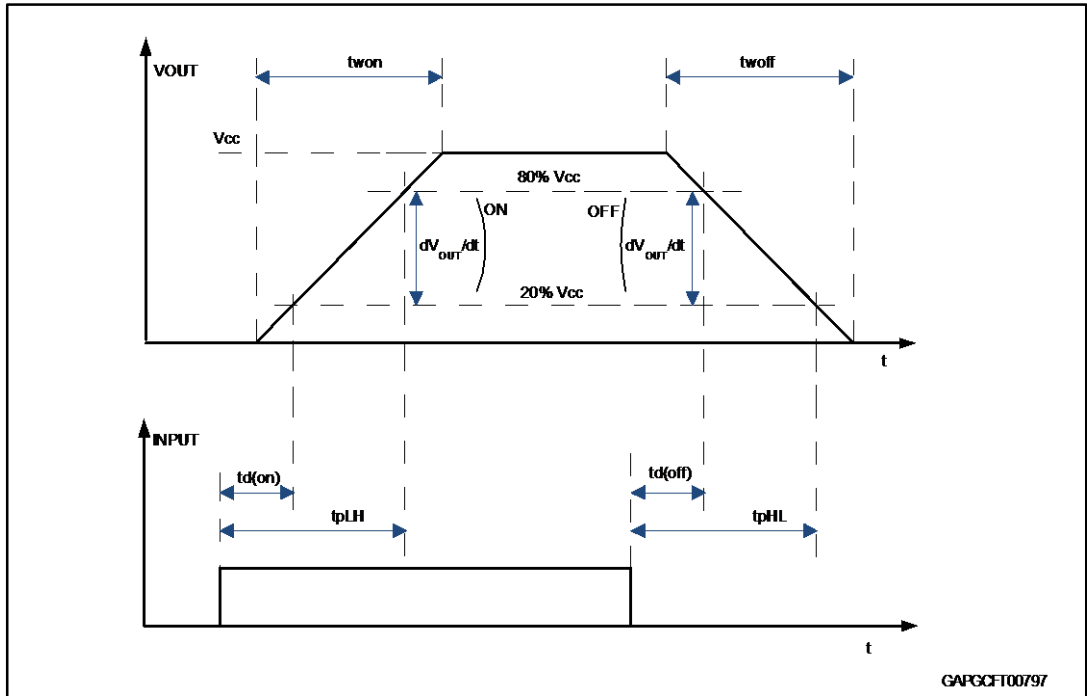


Figure 5: MultiSense timings (current sense mode)

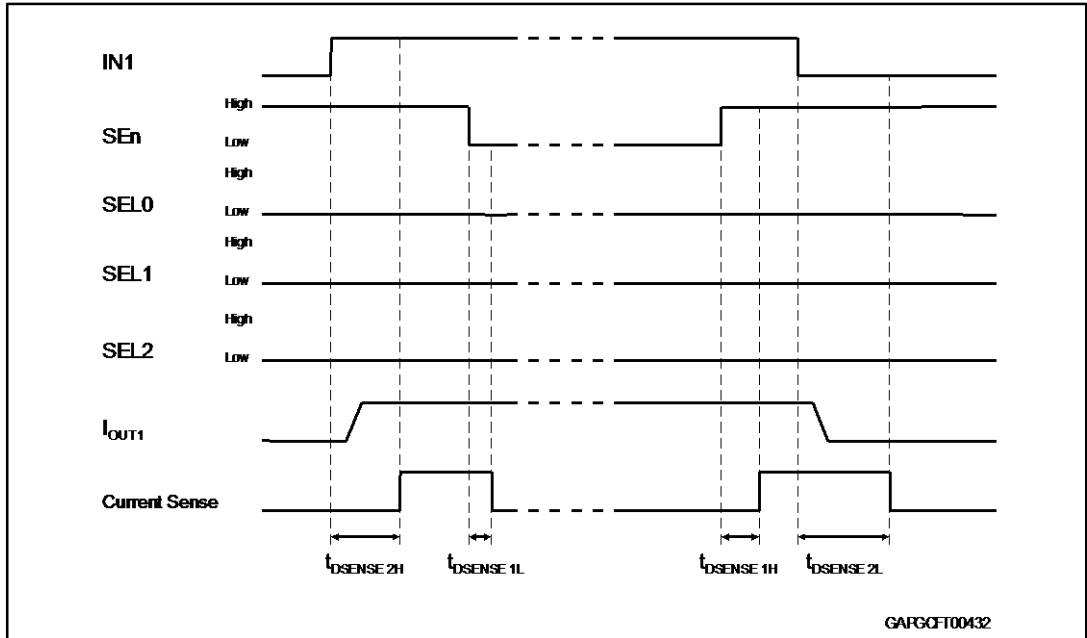
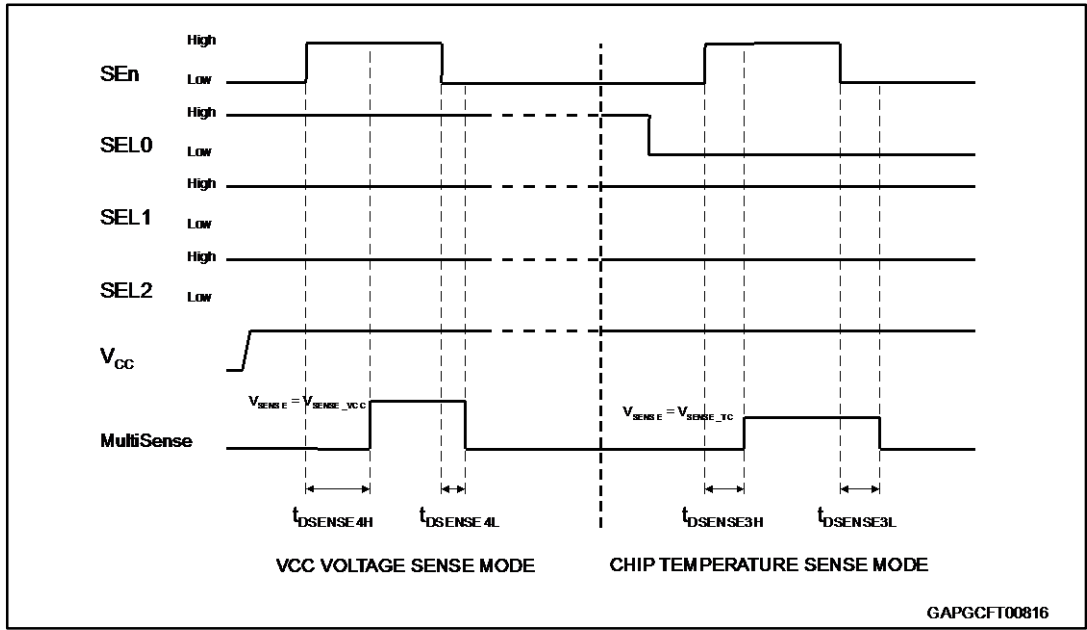
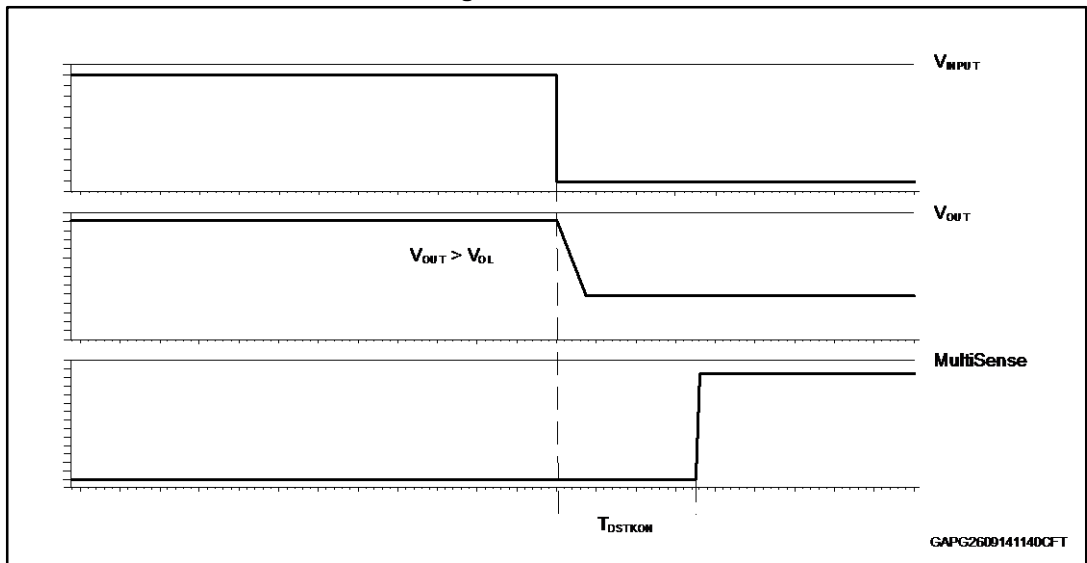


Figure 6: Multisense timings (chip temperature and VCC sense mode)



GAPGCFT00816

Figure 7: TDSKON



GAPG2600141140CFT

2.3.2 Bulb mode (default)

Table 9: Power section in Bulb Mode

| 7 V < V _{CC} < 28 V; -40 °C < T _j < 150 °C, unless otherwise specified | | | | | | |
|--|--|---|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| R _{ON_0,1,2,3_BULB} | On-state resistance in Bulb Mode Ch0, Ch1, Ch2 and Ch3 | I _{OUT} = 2.5 A; T _j = 25°C | | 40 | | mΩ |
| | | I _{OUT} = 2.5 A; T _j = 150°C | | | 80 | |

| 7 V < V _{CC} < 28 V; -40 °C < T _j < 150 °C, unless otherwise specified | | | | | | |
|--|---|---|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| | | I _{OUT} = 2.5 A; V _{CC} = 4 V; T _j = 25°C | | | 60 | |
| R _{ON_REV_0,1,2,3} | On-state resistance in Reverse Battery Ch0, Ch1, Ch2 and Ch3 | V _{CC} = -13V; I _{OUT} = -2.5A; T _j = 25°C | | 40 | | mΩ |
| I _{LIMH_0,1,2,3_BULB} ⁽¹⁾ | DC short circuit current in Bulb Mode Ch0, Ch1, Ch2 and Ch3 | V _{CC} = 13 V | 24 | 34 | 48 | A |
| | | 4 V < V _{CC} < 18 V ⁽²⁾ | | | 48 | |
| I _{LIML_0,1,2,3_BULB} | Short circuit current during thermal cycling in Bulb Mode Ch0, Ch1, Ch2 and Ch3 | V _{CC} = 13 V; T _R < T _j < T _{TSD} | | 9 | | |
| V _{ON_0,1,2,3_BULB} | Output voltage drop limitation in Bulb Mode Ch0, Ch1, Ch2 and Ch3 | I _{OUT} = 0.25 A | | 20 | | mV |

Notes:

(1)Parameter guaranteed by an indirect test sequence.

(2)Parameter guaranteed by design and characterization; not subject to production test.

Table 10: Switching in Bulb Mode

| V _{CC} = 13 V; -40 °C < T _j < 150 °C, unless otherwise specified | | | | | | |
|--|--|------------------------|------|------|---------------------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| Channel 0, 1, 2 and 3 | | | | | | |
| t _{d(on)_0,1,2,3} ⁽¹⁾ | Turn-on delay time at T _j = 25 °C | R _L = 5.2 Ω | 10 | 60 | 120 | μs |
| t _{d(off)_0,1,2,3} ⁽¹⁾ | Turn-off delay time at T _j = 25 °C | R _L = 5.2 Ω | 10 | 50 | 100 | |
| (dV _{OUT} /dt) _{on_0,1,2,3} ⁽¹⁾ | Turn-on voltage slope at T _j = 25 °C | R _L = 5.2 Ω | 0.1 | 0.5 | 0.7 | V/μs |
| (dV _{OUT} /dt) _{off_0,1,2,3} ⁽¹⁾ | Turn-off voltage slope at T _j = 25 °C | R _L = 5.2 Ω | 0.1 | 0.5 | 0.7 | |
| W _{ON_0,1,2,3} | Switching energy losses at turn-on (t _{won}) | R _L = 5.2 Ω | — | 0.2 | 0.52 ⁽²⁾ | mJ |
| W _{OFF_0,1,2,3} | Switching energy losses at turn-off (t _{woff}) | R _L = 5.2 Ω | — | 0.2 | 0.5 ⁽²⁾ | mJ |
| t _{SKEW_0,1,2,3} ⁽¹⁾ | Differential pulse skew (t _{PHL} - t _{PLH}) | R _L = 5.2 Ω | -65 | -15 | 35 | μs |

Notes:

(1)See [Figure 4: "Switching times and Pulse skew"](#).

(2)Parameter guaranteed by design and characterization, not subject to production test.

Table 11: MultiSense in Bulb Mode

| 7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C | | | | | | |
|--|--|--|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| Current sense characteristics | | | | | | |
| Channel 0, 1, 2 and 3 | | | | | | |
| K _{OL_CH0,1_B} | I _{OUT} /I _{SENSE} | I _{OUT} = 10 mA; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | 430 | | | |
| K _{OL_CH2,3_B} | I _{OUT} /I _{SENSE} | I _{OUT} = 10 mA; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | 430 | | | |
| dK _{cal} /K _{cal} ⁽¹⁾⁽²⁾ | Current sense ratio drift at calibration point | I _{CAL} = 30 mA; I _{OUT} = 10 mA to 50 mA; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | -35 | | 35 | % |
| K _{LED_CH0,1_B} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.05 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | 720 | 1440 | 2160 | |
| K _{LED_CH2,3_B} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.05 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | 720 | 1440 | 2160 | |
| K _{0_CH0,1_B} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.25 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | 930 | 1550 | 2170 | |
| K _{0_CH2,3_B} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.25 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | 930 | 1550 | 2170 | |
| dK ₀ /K ₀ ⁽¹⁾⁽²⁾ | Current sense ratio drift | I _{OUT} = 0.25 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | -20 | | 20 | % |
| K _{1_CH0,1_B} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.5 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | 1110 | 1590 | 2070 | |
| K _{1_CH2,3_B} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.5 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | 1085 | 1550 | 2015 | |
| dK ₁ /K ₁ ⁽¹⁾⁽²⁾ | Current sense ratio drift | I _{OUT} = 0.5 A; V _{SENSE} = 4V; V _{SEN} = 5 V | -15 | | 15 | % |
| K _{2_CH0,1_B} | I _{OUT} /I _{SENSE} | I _{OUT} = 2 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | 1160 | 1450 | 1740 | |
| K _{2_CH2,3_B} | I _{OUT} /I _{SENSE} | I _{OUT} = 2 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | 1130 | 1410 | 1690 | |
| dK ₂ /K ₂ ⁽¹⁾⁽²⁾ | Current sense ratio drift | I _{OUT} = 2 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | -10 | | 10 | % |

| 7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C | | | | | | |
|--|---|--|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| K _{3_CH0,1_B} | I _{OUT} /I _{SENSE} | I _{OUT} = 6 A; V _{SENSE} = 4 V; V _{SEn} = 5 V | 1295 | 1440 | 1585 | |
| K _{3_CH2,3_B} | I _{OUT} /I _{SENSE} | I _{OUT} = 6 A; V _{SENSE} = 4 V; V _{SEn} = 5 V | 1260 | 1400 | 1540 | |
| dK ₃ /K ₃ ⁽¹⁾⁽²⁾ | Current sense ratio drift | I _{OUT} = 6 A; V _{SENSE} = 4 V; V _{SEn} = 5 V | -5 | | 5 | % |
| MultiSense timings (Current Sense mode see Figure 5: "MultiSense timings (current sense mode)") | | | | | | |
| Channel 0, 1, 2 and 3 | | | | | | |
| t _{DSENSE1H} | Current sense settling time from rising edge of SE _n | V _{IN} = 5 V; V _{SEn} = 0 V to 5 V; R _{SENSE} = 1 kΩ; R _L = 5.2 Ω | | | 60 | μs |
| t _{DSENSE1L} | Current sense disable delay time from falling edge of SE _n | V _{SEn} = 5 V to 0 V; R _{SENSE} = 1 kΩ; R _L = 5.2 Ω | | 5 | 20 | μs |
| t _{DSENSE2H} | Current sense settling time from rising edge of INPUT | V _{IN} = 0 V to 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 5.2 Ω | | 100 | 250 | μs |
| Δt _{DSENSE2H} | Current sense settling time from rising edge of I _{OUT} (dynamic response to a step change of I _{OUT}) | V _{IN} = 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 5.2 Ω | | | 100 | μs |
| t _{DSENSE2L} | Current sense turn-off delay time from falling edge of INPUT | V _{IN} = 5 V to 0 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 5.2 Ω | | 50 | 250 | μs |

Notes:

⁽¹⁾Parameter specified by design; not subject to production test.

⁽²⁾All values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

Figure 8: Bulb Mode - IOUT/ISENSE versus IOUT

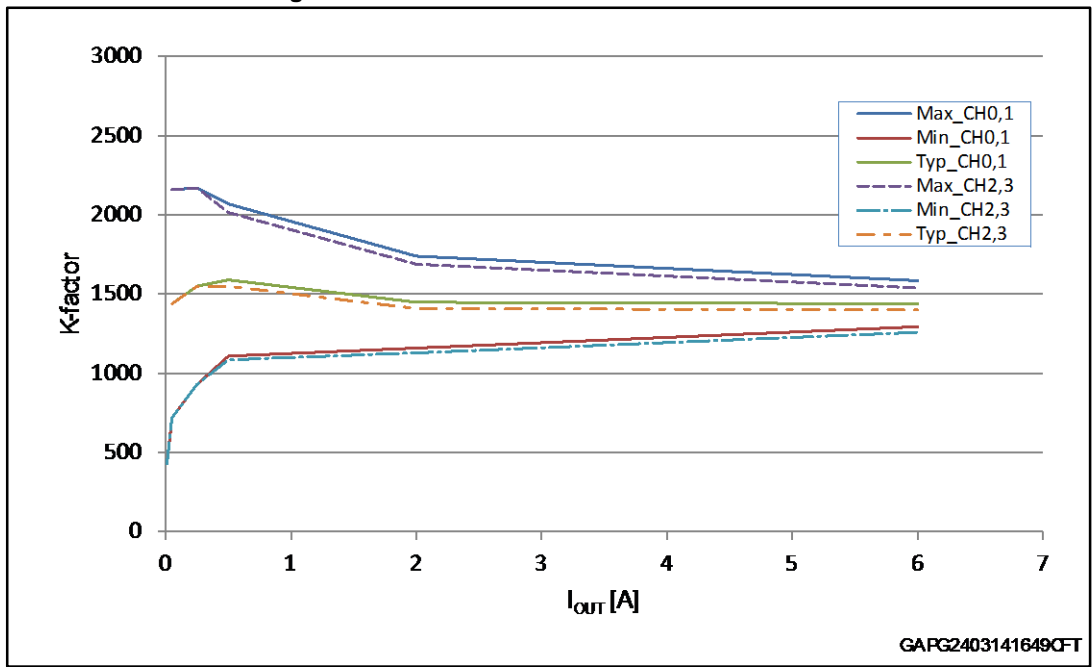
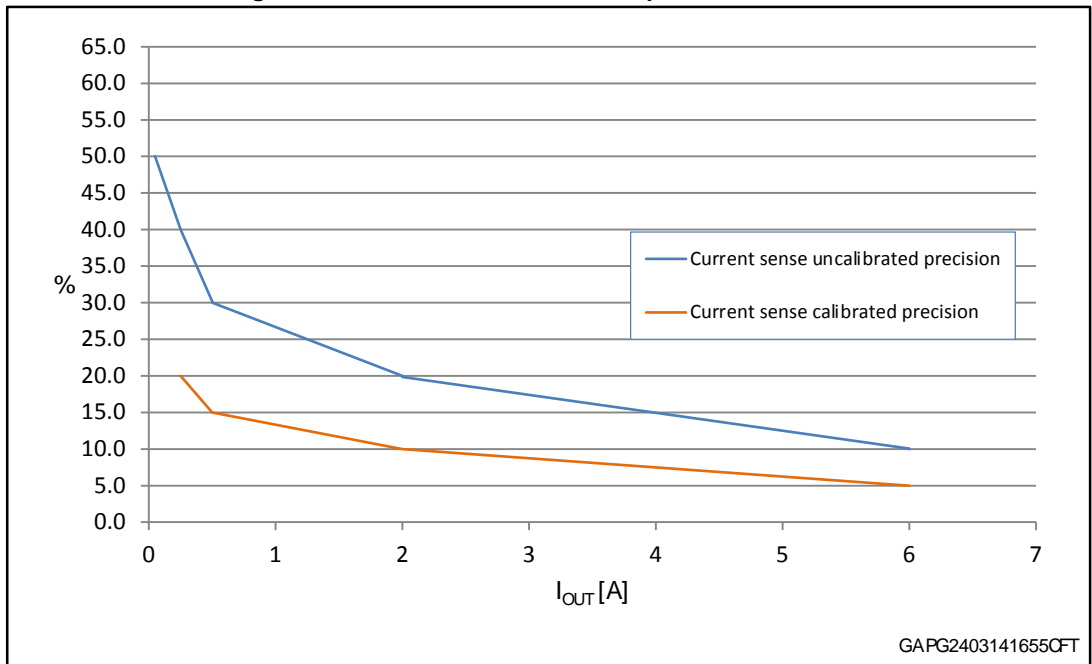


Figure 9: Bulb Mode - current sense precision vs. IOUT



2.3.3 Electrical characteristics curves - Bulb Mode

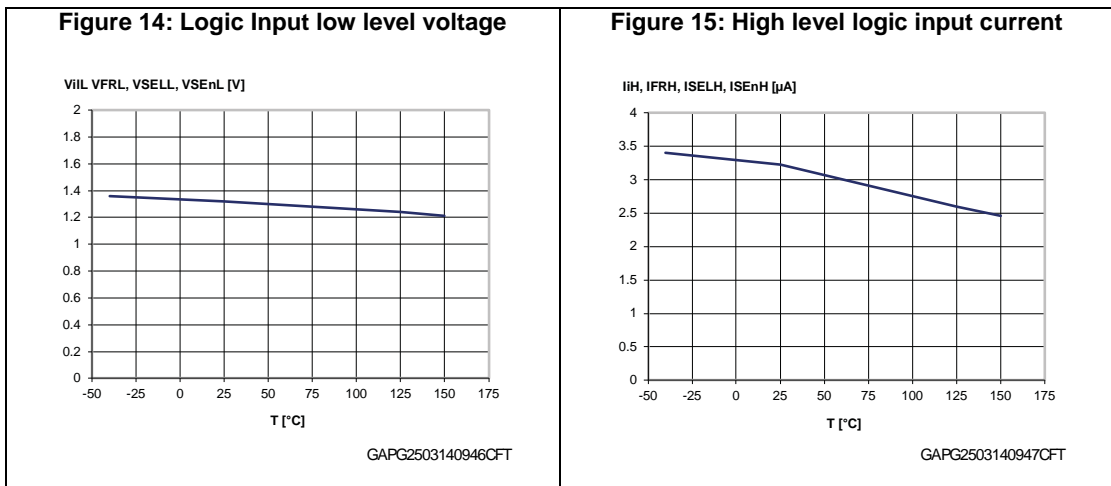
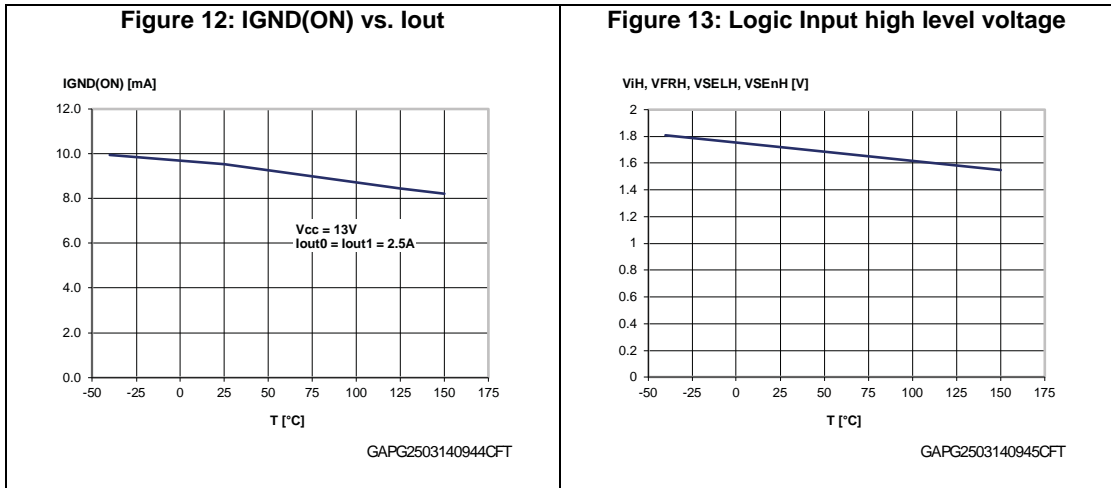
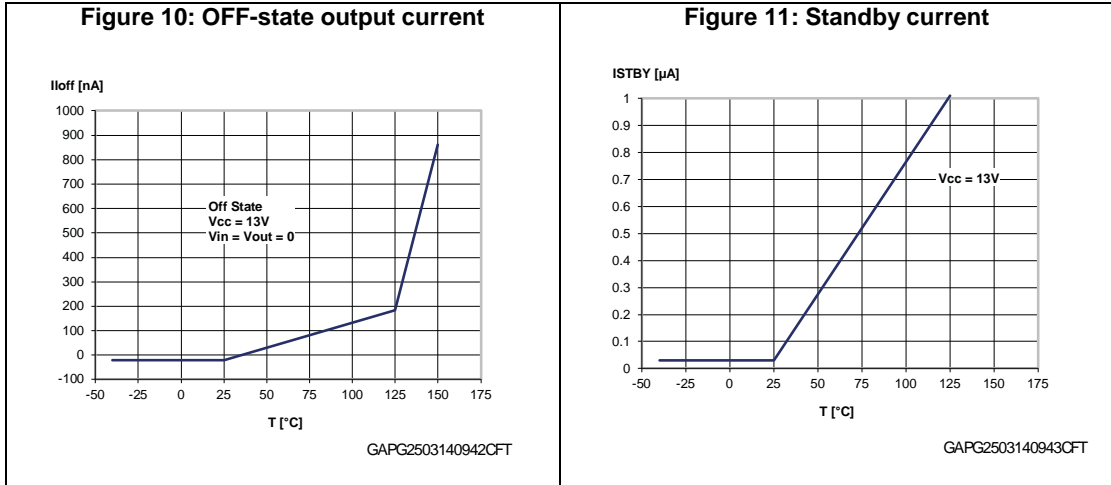
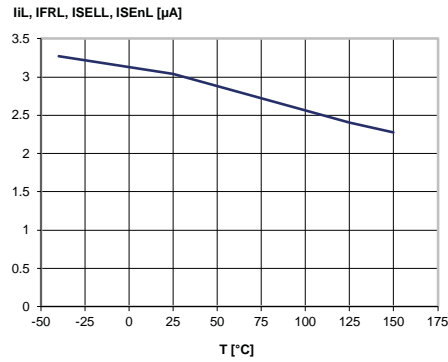
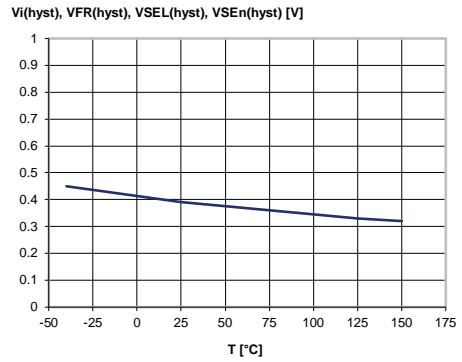


Figure 16: Low level logic input current



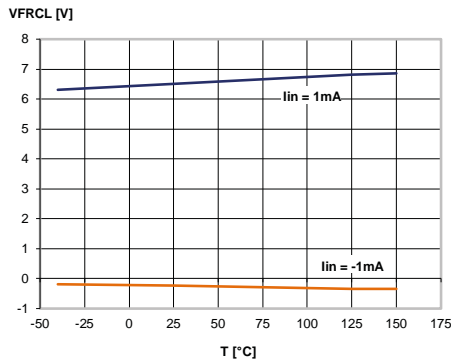
GAPG2503140948CFT

Figure 17: Logic Input hysteresis voltage



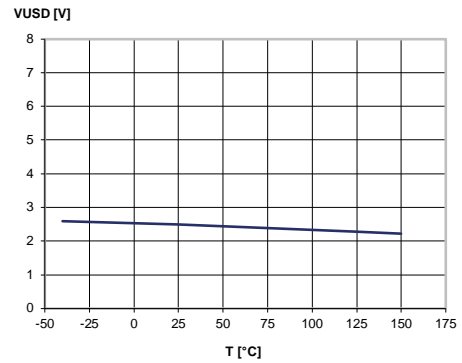
GAPG2503140949CFT

Figure 18: FaultRST Input clamp voltage



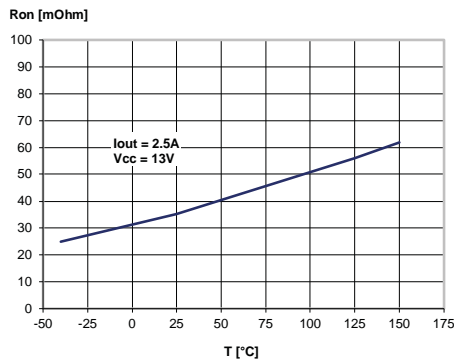
GAPG2503140950CFT

Figure 19: Undervoltage shutdown



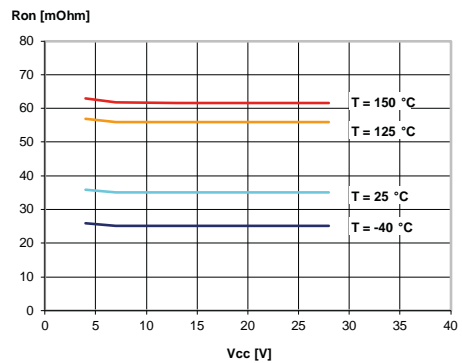
GAPG2503140951CFT

Figure 20: On-state resistance vs. Tcase

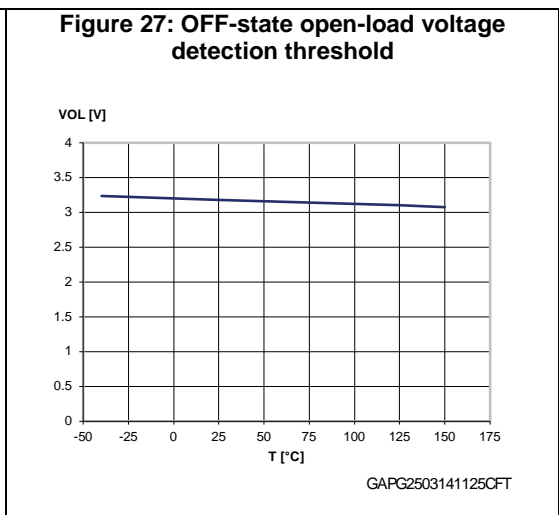
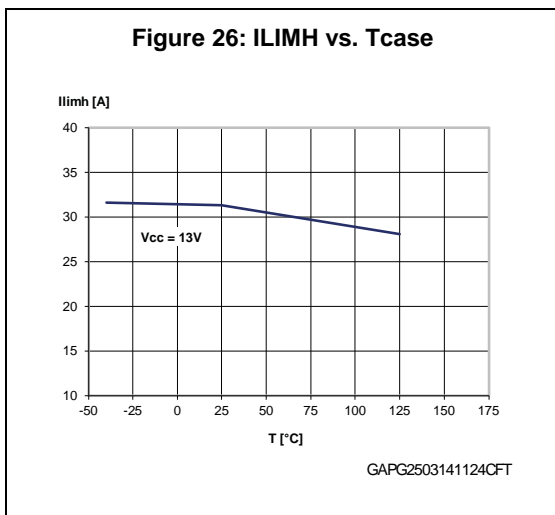
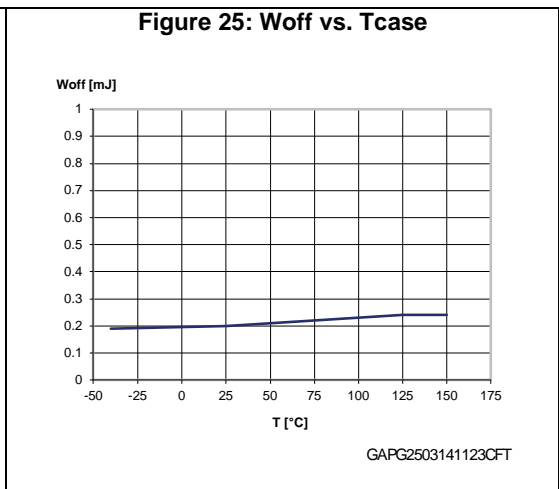
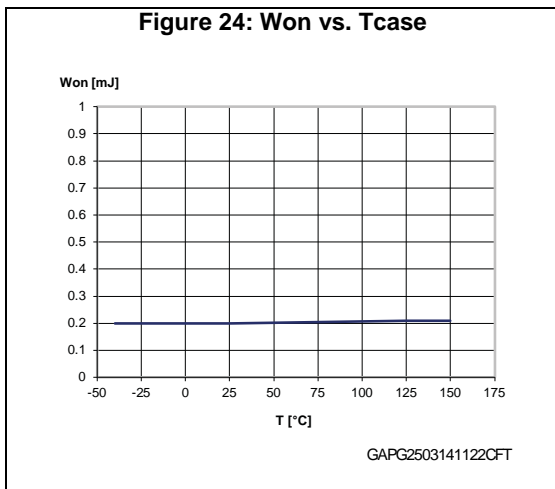
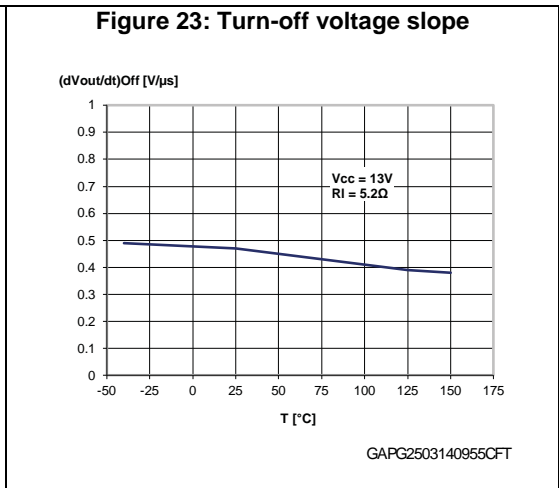
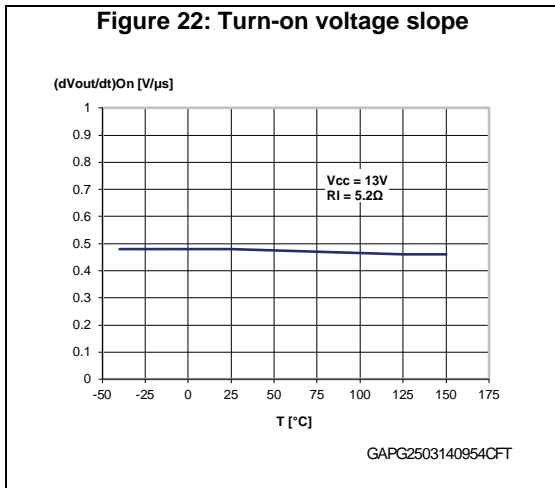


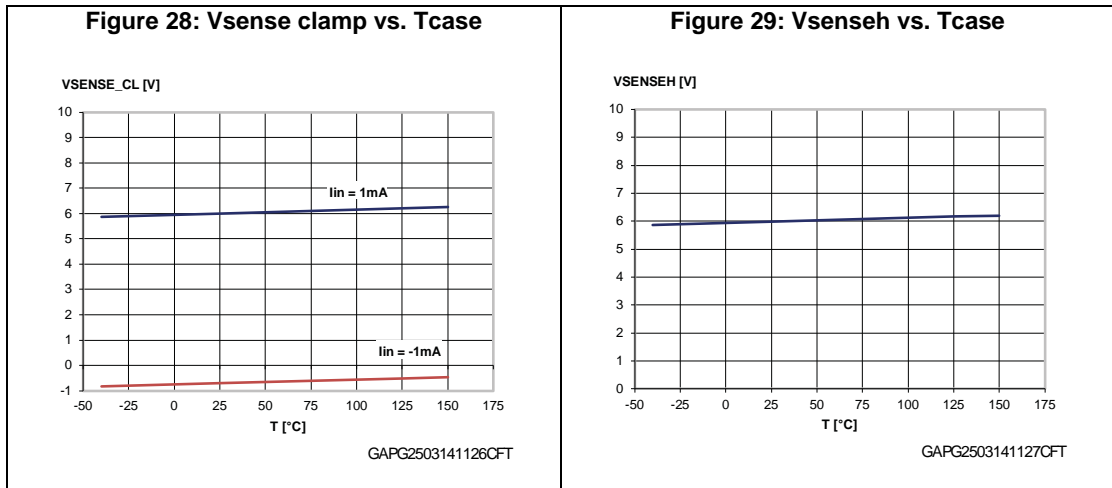
GAPG2503140952CFT

Figure 21: On-state resistance vs. VCC



GAPG2503140953CFT





2.3.4 LED Mode (Channel 0 and 1)

Table 12: Switching in LED Mode

| V _{CC} = 13 V; -40 °C < T _j < 150 °C, unless otherwise specified | | | | | | |
|--|--|-------------------------|------|-------|---------------------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| t _{d(on)_0,1_LED} ⁽¹⁾ | Turn-on delay time at T _j = 25 °C | R _L = 22.8 Ω | 10 | 65 | 120 | μs |
| t _{d(off)_0,1_LED} ⁽¹⁾ | Turn-off delay time at T _j = 25 °C | R _L = 22.8 Ω | 10 | 40 | 100 | |
| (dV _{OUT} /dt) _{on_0,1_LED} ⁽¹⁾ | Turn-on voltage slope at T _j = 25 °C | R _L = 22.8 Ω | 0.2 | 0.5 | 0.8 | V/μs |
| (dV _{OUT} /dt) _{off_0,1_LED} ⁽¹⁾ | Turn-off voltage slope at T _j = 25 °C | R _L = 22.8 Ω | 0.1 | 0.5 | 0.7 | |
| W _{ON_0,1_LED} | Switching energy losses at turn-on (t _{won}) | R _L = 22.8 Ω | — | 0.04 | 0.1 ⁽²⁾ | mJ |
| W _{OFF_0,1_LED} | Switching energy losses at turn-off (t _{woff}) | R _L = 22.8 Ω | — | 0.045 | 0.11 ⁽²⁾ | mJ |
| t _{SKEW_0,1_LED} ⁽¹⁾ | Differential Pulse skew (t _{PHL} - t _{PLH}) | R _L = 22.8 Ω | -75 | -25 | 25 | μs |

Notes:

⁽¹⁾See [Figure 4: "Switching times and Pulse skew"](#).

⁽²⁾Parameter guaranteed by design and characterization, not subject to production test.

Table 13: Power section in LED Mode

| 7 V < V _{CC} < 28 V; -40 °C < T _j < 150 °C, unless otherwise specified | | | | | | |
|--|---|--|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| R _{ON_0,1_LED} | On-state resistance in LED Mode Ch0 and Ch1 | I _{OUT} = 0.57 A; T _j = 25°C | | 140 | | mΩ |
| | | I _{OUT} = 0.57 A; T _j = 150°C | | | 280 | |

| 7 V < V _{CC} < 28 V; -40 °C < T _j < 150 °C, unless otherwise specified | | | | | | |
|--|---|---|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| | | I _{OUT} = 0.57 A; V _{CC} = 5 V; T _j = 25°C | | | 210 | |
| I _{LIMH_0,1_LED} ⁽¹⁾ | DC short circuit current in Bulb Mode Ch0 and Ch1 | V _{CC} = 13 V 4 V < V _{CC} < 18 V ⁽²⁾ | 5.5 | 8 | 11 | A |
| I _{LIML_0,1_LED} | Short circuit current during thermal cycling in Bulb Mode Ch0 and Ch1 | V _{CC} = 13 V; T _R < T _j < T _{TSD} | | 2 | | |
| V _{ON_0,1_LED} | Output voltage drop limitation in LED Mode Ch0 and Ch1 | I _{OUT} = 0.07 A | | 20 | | mV |

Notes:

(1)Parameter guaranteed by an indirect test sequence.

(2)Parameter guaranteed by design and characterization; not subject to production test.

Table 14: MultiSense in LED Mode

| 7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C | | | | | | |
|--|--|--|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| K _{OL} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.01 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | 120 | | | |
| dK _{cal} /K _{cal} ⁽¹⁾⁽²⁾ | Current sense ratio drift at calibration point | I _{cal} = 17.5 mA; I _{OUT} = 10 mA to 25 mA; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | -30 | | 30 | % |
| K _{LED} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.025 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | 150 | 380 | 610 | |
| dK _{LED} /K _{LED} ⁽¹⁾⁽²⁾ | Current sense ratio drift | I _{OUT} = 0.025 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | -25 | | 25 | % |
| K _{0_CH0,1_L} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.15 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | 240 | 405 | 570 | |
| dK ₀ /K ₀ ⁽¹⁾⁽²⁾ | Current sense ratio drift | I _{OUT} = 0.15 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | -15 | | 15 | % |
| K _{1_CH0,1_L} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.7 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | 300 | 380 | 460 | |
| dK ₁ /K ₁ ⁽¹⁾⁽²⁾ | Current sense ratio drift | I _{OUT} = 0.7 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | -8 | | 8 | % |
| MultiSense timings (Current Sense mode - see Figure 5: "MultiSense timings (current sense mode)") | | | | | | |

| 7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C | | | | | | |
|--|---|---|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| t _{DSENSE1H} | Current sense settling time from rising edge of SEn | V _{IN} = 5 V; V _{SEn} = 0 V to 5 V; R _{SENSE} = 1 kΩ; R _L = 22.8 Ω | | | 60 | μs |
| t _{DSENSE1L} | Current sense disable delay time from falling edge of SEn | V _{SEn} = 5 V to 0 V; R _{SENSE} = 1 kΩ; R _L = 22.8 Ω | | 5 | 20 | μs |
| t _{DSENSE2H} | Current sense settling time from rising edge of INPUT | V _{IN} = 0 V to 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 22.8 Ω | | | 250 | μs |
| Δt _{DSENSE2H} | Current sense settling time from rising edge of I _{OUT} (dynamic response to a step change of I _{OUT}) | V _{IN} = 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 22.8 Ω | | | 100 | μs |
| t _{DSENSE2L} | Current sense turn-off delay time from falling edge of INPUT | V _{IN} = 5 V to 0 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 22.8 Ω | | 50 | 250 | μs |

Notes:

- (1)Parameter specified by design; not subject to production test.
- (2)All values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

Figure 30: LED Mode - I_{OUT}/I_{SENSE} versus I_{OUT}

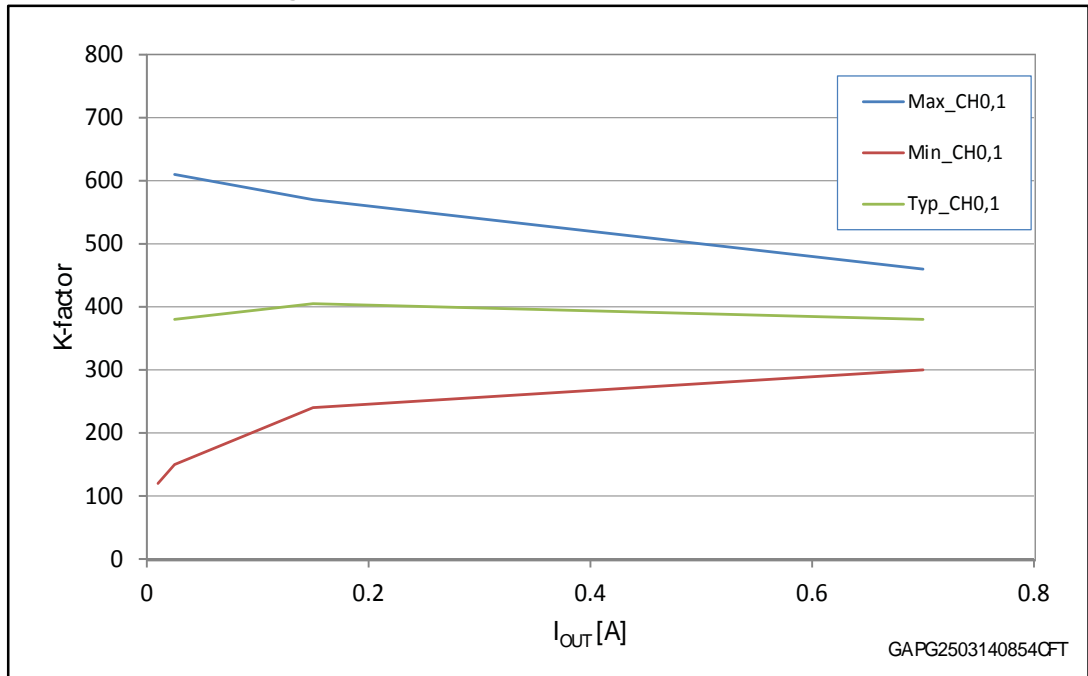
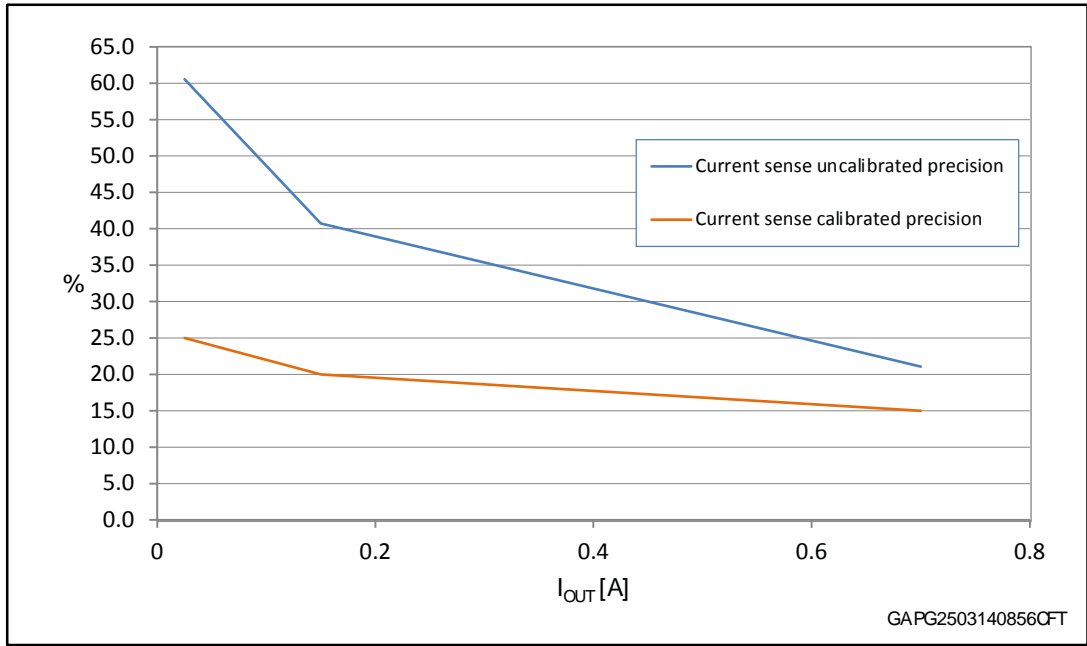


Figure 31: LED Mode - current sense precision vs. IOU



2.3.5 Electrical characteristics curves - LED mode

Figure 32: On-state resistance vs. Tcase

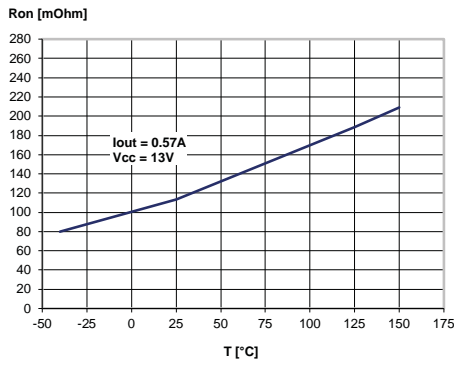


Figure 33: On-state resistance vs. VCC

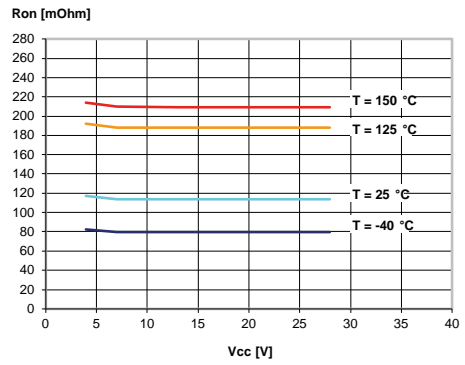


Figure 34: Turn-on voltage slope

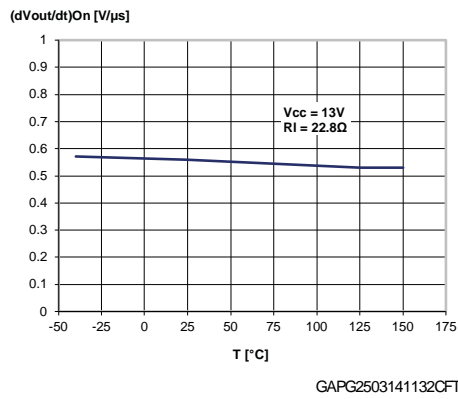


Figure 35: Turn-off voltage slope

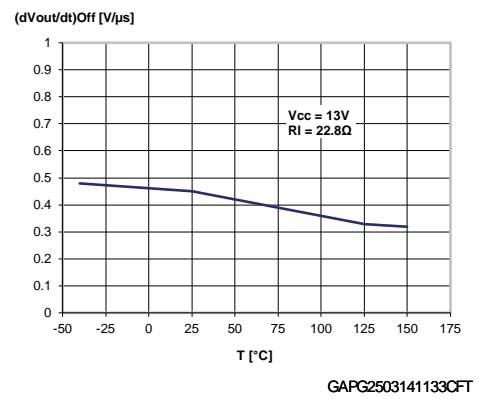


Figure 36: Won vs. Tcase

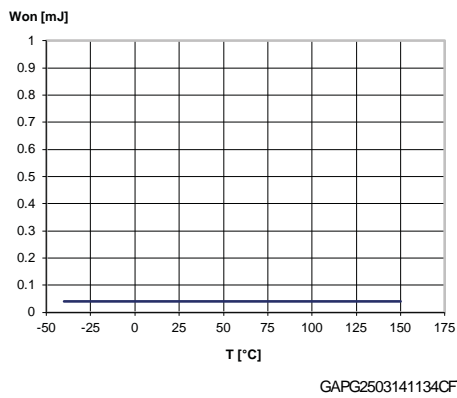


Figure 37: Woff vs. Tcase

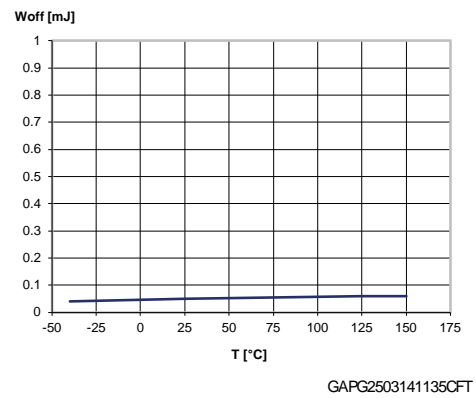
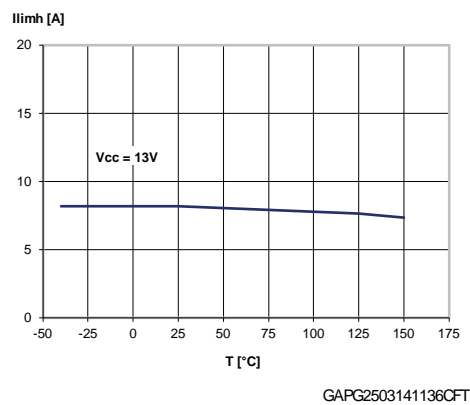


Figure 38: ILIMH vs. Tcase



2.3.6 Truth tables

Table 15: Truth table

| Mode | Conditions | IN _x | FR | SEn | SEL _x | OUT _x | MultiSense | Comments |
|-------------------------|---|-----------------|----|--------------------|------------------|------------------|--------------------|--|
| Standby | All logic inputs low | L | L | L | L | L | Hi-Z | Low quiescent current consumption |
| Normal | Nominal load connected; T _j < 150°C | L | X | See ⁽¹⁾ | | L | See ⁽¹⁾ | |
| | | H | L | | | H | See ⁽¹⁾ | Outputs configured for auto-restart |
| | | H | H | | | H | See ⁽¹⁾ | Outputs configured for Latch-off |
| Overload | Overload or short to GND causing: T _j > T _{TSO} or ΔT _j > ΔT _{j,SD} | L | X | See ⁽¹⁾ | | L | See ⁽¹⁾ | |
| | | H | L | | | H | See ⁽¹⁾ | Output cycles with temperature hysteresis |
| | | H | H | | | L | See ⁽¹⁾ | Output latches-off |
| Under-voltage | V _{CC} < V _{USD} (falling) | X | X | X | X | L L | Hi-Z Hi-Z | Re-start when V _{CC} > V _{USD} + V _{USDhyst} (rising) |
| OFF-state diagnostics | Short to V _{CC} | L | X | See ⁽¹⁾ | | H | See ⁽¹⁾ | |
| | Open load | L | X | | | H | See ⁽¹⁾ | External pull-up |
| Negative output voltage | Inductive loads turn off | L | X | See ⁽¹⁾ | | < 0V | See ⁽¹⁾ | |

Notes:

⁽¹⁾Refer to [Table 16: "MultiSense multiplexer addressing"](#)

Table 16: MultiSense multiplexer addressing

| SEn | SEL ₂ | SEL ₁ | SEL ₀ | MUX channel | MultiSense output | | | |
|-----|------------------|------------------|------------------|-------------------------|---|---|---|-----------------|
| | | | | | Normal mode | Overload | OFF-state diag. ⁽¹⁾ | Negative output |
| L | X | X | X | | Hi-Z | | | |
| H | L | L | L | Channel 0 diagnostic | I _{SENSE} = 1/K * I _{OUT0} | V _{SENSE} = V _{SENSEH} | V _{SENSE} = V _{SENSEH} | Hi-Z |
| H | L | L | H | Channel 1 diagnostic | I _{SENSE} = 1/K * I _{OUT1} | V _{SENSE} = V _{SENSEH} | V _{SENSE} = V _{SENSEH} | Hi-Z |
| H | L | H | L | Channel 2 diagnostic | I _{SENSE} = 1/K * I _{OUT2} | V _{SENSE} = V _{SENSEH} | V _{SENSE} = V _{SENSEH} | Hi-Z |
| H | L | H | H | Channel 3 diagnostic | I _{SENSE} = 1/K * I _{OUT3} | V _{SENSE} = V _{SENSEH} | V _{SENSE} = V _{SENSEH} | Hi-Z |
| H | H | L | L | T _{CHIP} Sense | V _{SENSE} = V _{SENSE_TC} | | | |
| H | H | L | H | V _{CC} Sense | V _{SENSE} = V _{SENSE_VCC} | | | |
| H | H | H | L | T _{CHIP} Sense | V _{SENSE} = V _{SENSE_TC} | | | |
| H | H | H | H | V _{CC} Sense | V _{SENSE} = V _{SENSE_VCC} | | | |

Notes:

⁽¹⁾In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic. Example 1: FR = 1; IN₀ = 0; OUT₀ = L (latched); MUX

channel = channel 0 diagnostic; Mutisense = 0. Example 2: FR = 1; IN₀ = 0; OUT₀ = latched, V_{OUT0} > V_{OL}; MUX
channel = channel 0 diagnostic; Mutisense = V_{SENSEH}

Table 17: Bulb/LED Mode Configuration

| LED ₁ | LED ₀ | Configuration | |
|------------------|------------------|---------------|-----------|
| | | Channel 1 | Channel 0 |
| L | L | Bulb | Bulb |
| L | H | Bulb | LED |
| H | L | LED | Bulb |
| H | H | LED | LED |

3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD} . According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remains off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (FaultRST = Low) or remains off (FaultRST = High).

3.3 Current limitation

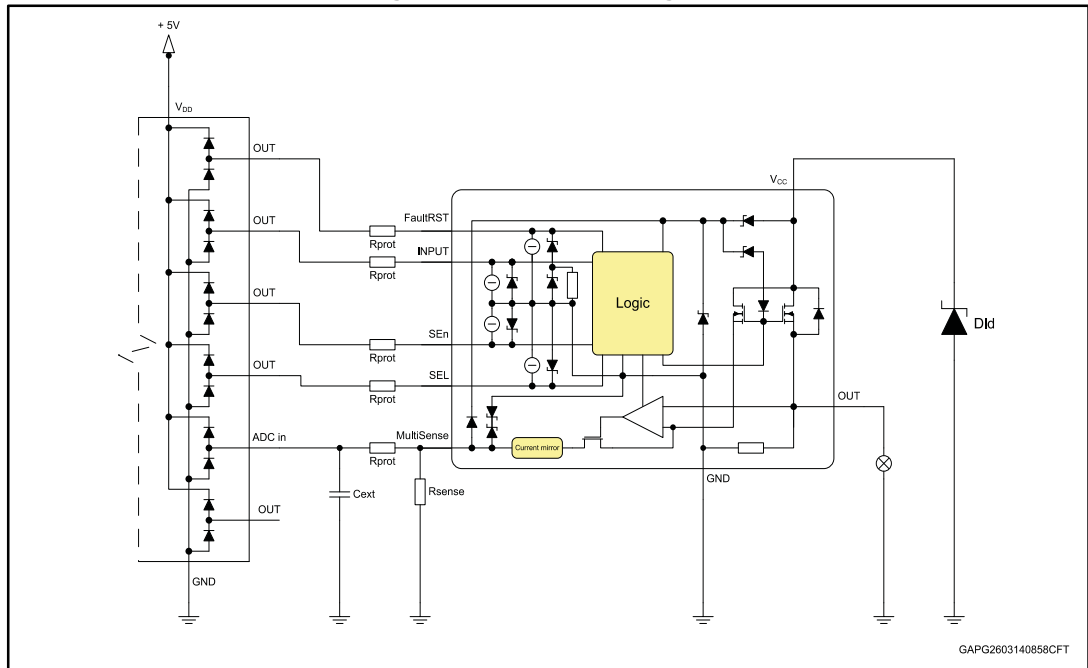
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH} , by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG} , allowing the inductor energy to be dissipated without damaging the device.

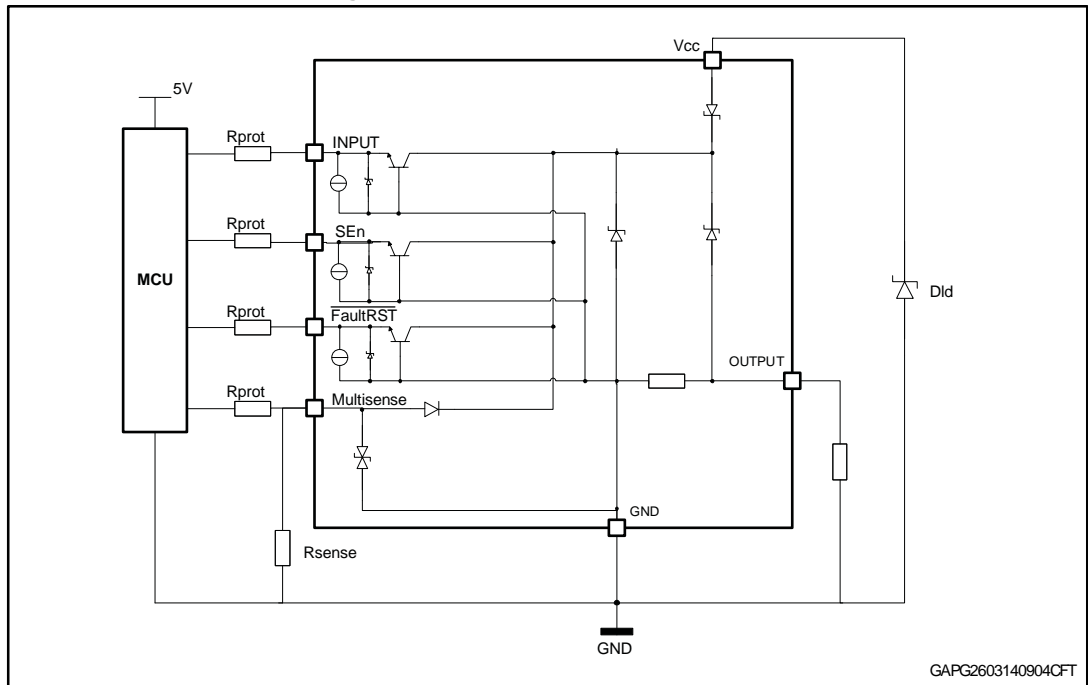
4 Application information

Figure 39: Application diagram



4.1 GND protection network against reverse battery

Figure 40: Simplified internal structure



The device does not need any external components to protect the internal logic in case of a reverse battery condition. The protection is provided by internal structures.

In addition, due to the fact that the output MOSFET turns on even in reverse battery mode, thus providing the same low ohmic path as in regular operating conditions, no additional power dissipation has to be considered.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in [Table 18: "ISO 7637-2 - electrical transient conduction along supply line"](#).

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

Table 18: ISO 7637-2 - electrical transient conduction along supply line

| Test Pulse 2011(E) | Test pulse severity level with Status II functional performance status | | Minimum number of pulses or test time | Burst cycle / pulse repetition time | | Pulse duration and pulse generator internal impedance |
|--|--|-------------|---------------------------------------|-------------------------------------|--------|---|
| | Level | $U_S^{(1)}$ | | min | max | |
| 1 | III | -112V | 500 pulses | 0,5 s | | 2ms, 10 Ω |
| 2a | III | +55V | 500 pulses | 0,2 s | 5 s | 50 μ s, 2 Ω |
| 3a | IV | -220V | 1h | 90 ms | 100 ms | 0.1 μ s, 50 Ω |
| 3b | IV | +150V | 1h | 90 ms | 100 ms | 0.1 μ s, 50 Ω |
| 4 ⁽²⁾ | IV | -7V | 1 pulse | | | 100ms, 0.01 Ω |
| Load dump according to ISO 16750-2:2010 | | | | | | |
| Test B ⁽³⁾ | | 40V | 5 pulse | 1 min | | 400ms, 2 Ω |

Notes:

⁽¹⁾ U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

⁽²⁾Test pulse from ISO 7637-2:2004(E).

⁽³⁾With 40 V external suppressor referred to ground ($-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$).

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation

$$V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -150 \text{ V}$; $I_{latchup} \geq 20 \text{ mA}$; $V_{OH\mu C} \geq 4.5 \text{ V}$

$7.5 \text{ k}\Omega \leq R_{prot} \leq 140 \text{ k}\Omega$.

Recommended values: $R_{prot} = 15 \text{ k}\Omega$

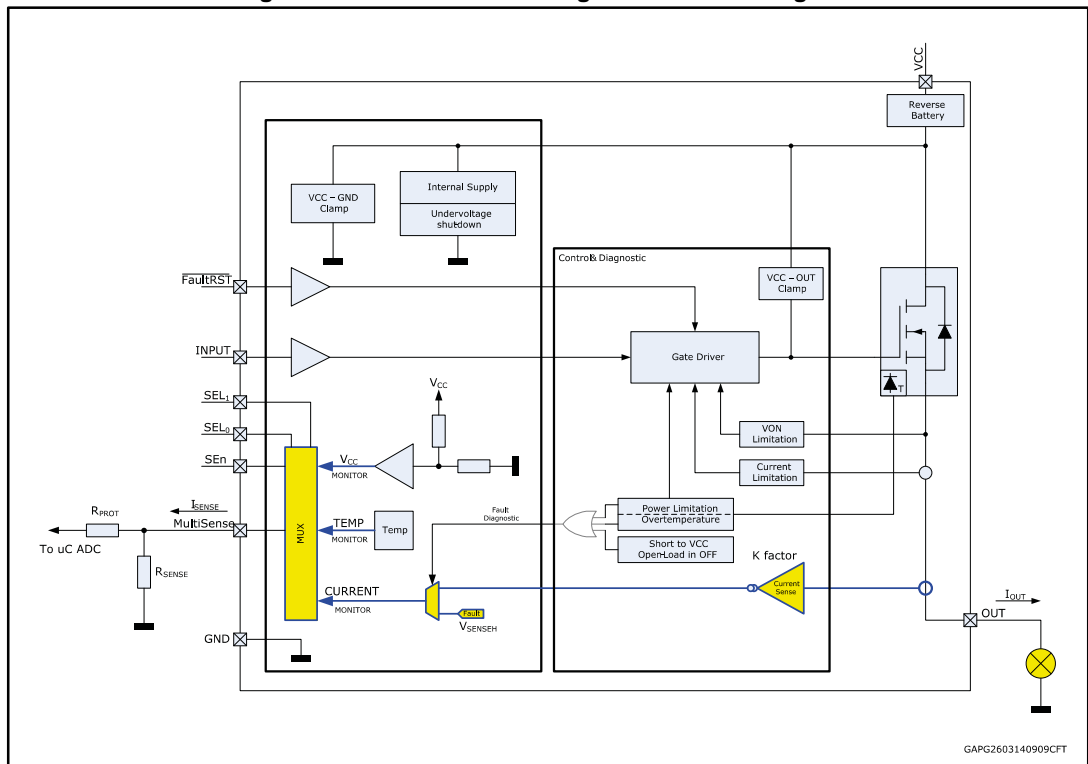
4.4 Multisense - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (MultiSense) delivering the following signals:

- Current monitor: current mirror of channel output current
- V_{CC} monitor: voltage proportional to V_{CC}
- T_{CASE} : voltage proportional to chip temperature

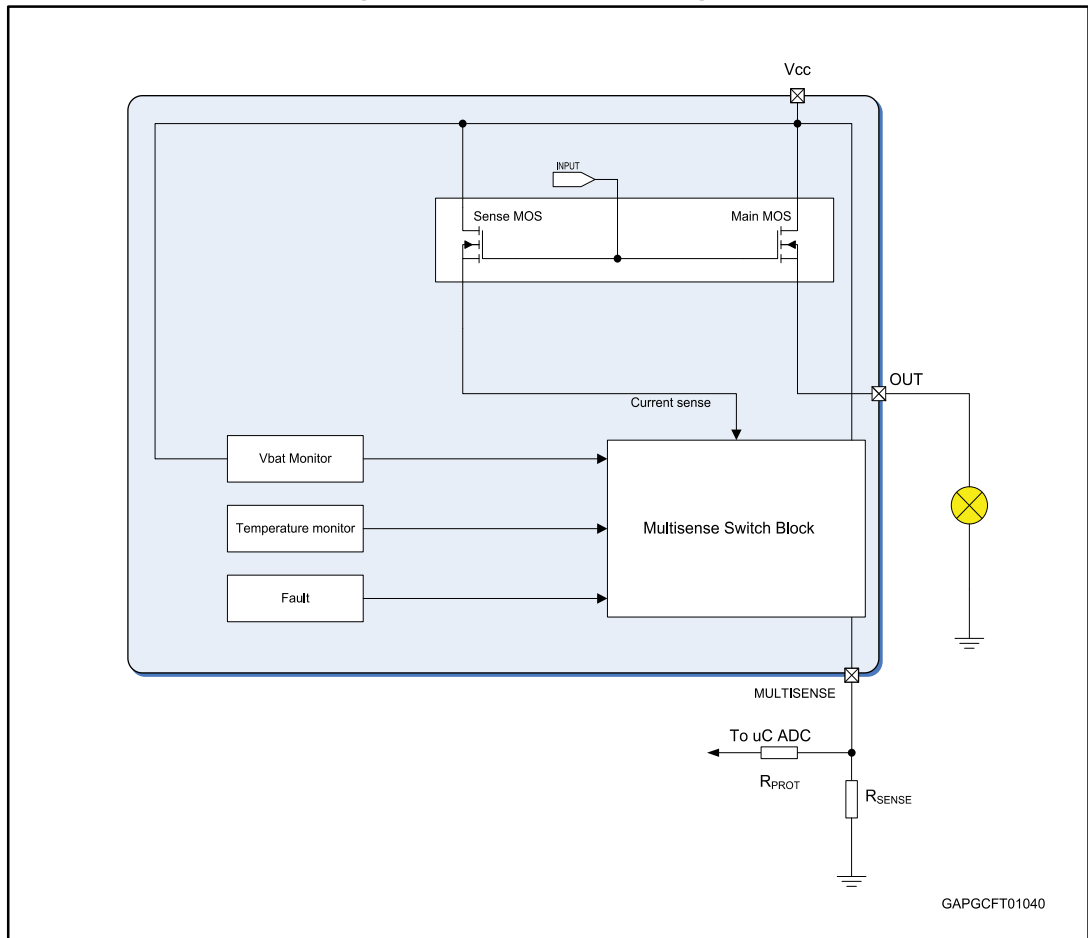
Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in *MultiSense multiplexer addressing Table*.

Figure 41: MultiSense and diagnostic – block diagram



4.4.1 Principle of Multisense signal generation

Figure 42: MultiSense block diagram



Current monitor

When current mode is selected via MultiSense, this output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to a known ratio named **K**
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE} , can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE} , allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by MultiSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE} : $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is the voltage measurable on R_{SENSE} resistor
- I_{SENSE} is the current provided from MultiSense pin in current output mode

- I_{OUT} is the current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying the ratio between I_{OUT} and I_{SENSE} .

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the MultiSense pin which is switched to a “current limited” voltage source, V_{SENSEH} .

In any case, the current sourced by the MultiSense in this condition is limited to I_{SENSEH} .

The typical behavior in case of overload or hard short circuit is shown in *Waveforms section*.

Figure 43: Analogue HSD – open-load detection in off-state

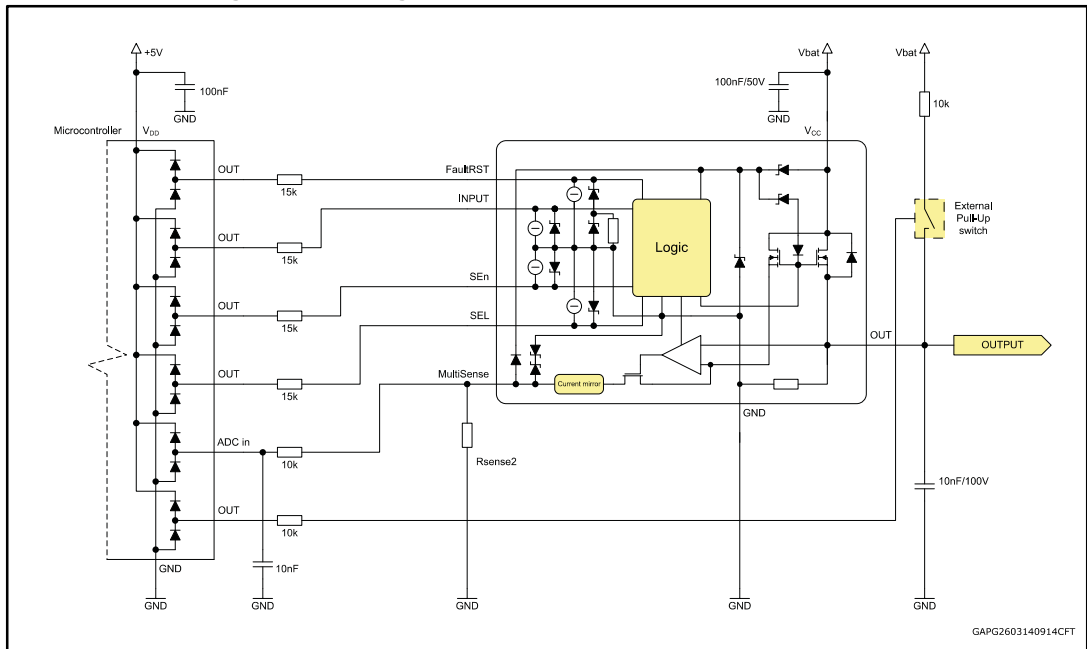


Figure 44: Open-load / short to VCC condition

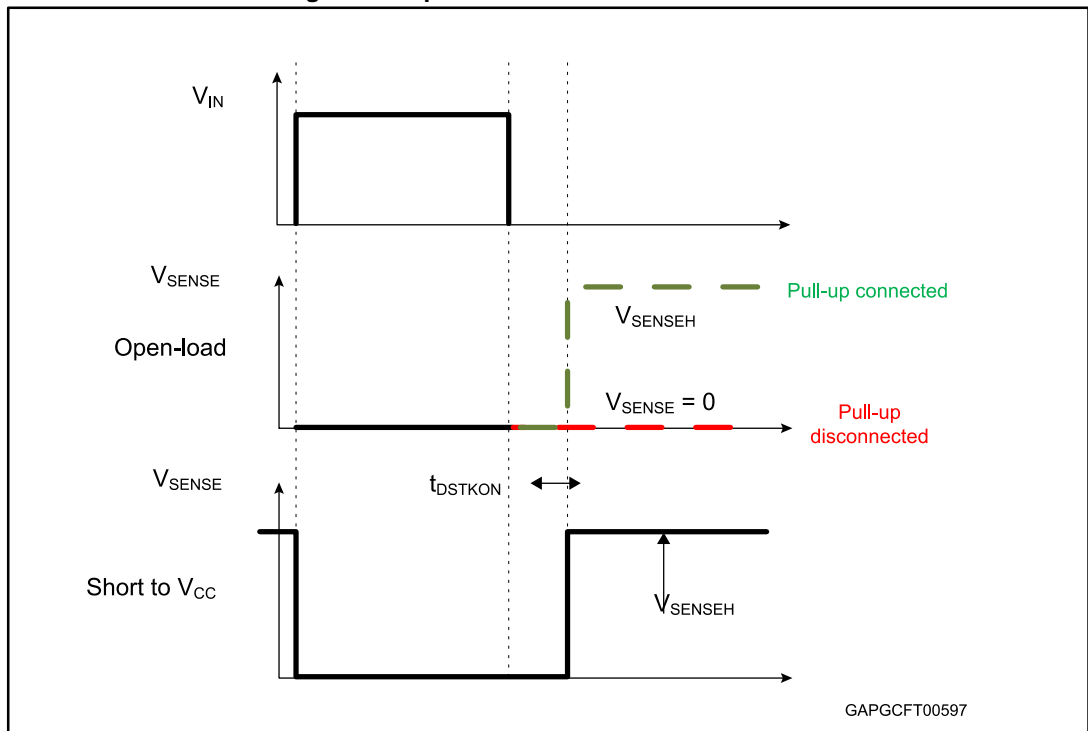


Table 19: MultiSense pin levels in off-state

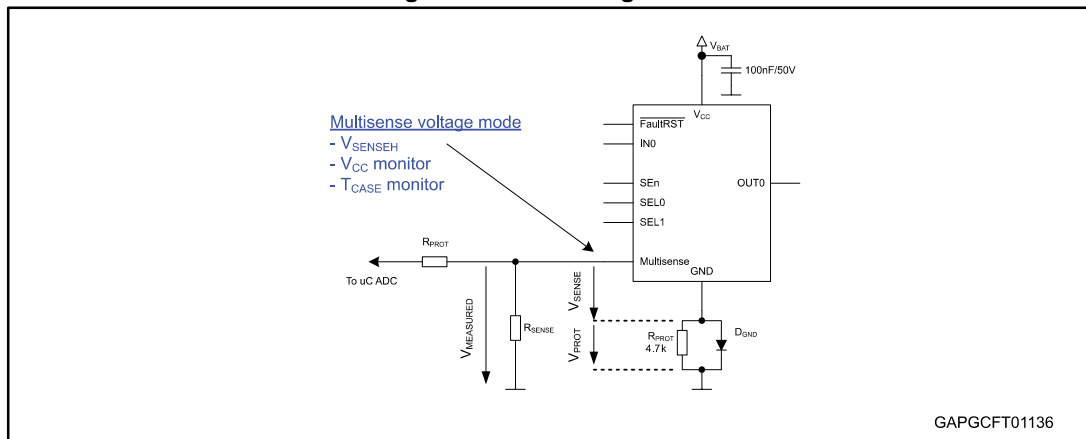
| Condition | Output | MultiSense | SEn |
|-------------------|--------------------|--------------|-----|
| Open-load | $V_{OUT} > V_{OL}$ | Hi-Z | L |
| | | V_{SENSEH} | H |
| | $V_{OUT} < V_{OL}$ | Hi-Z | L |
| | | 0 | H |
| Short to V_{CC} | $V_{OUT} > V_{OL}$ | Hi-Z | L |
| | | V_{SENSEH} | H |
| Nominal | $V_{OUT} < V_{OL}$ | Hi-Z | L |
| | | 0 | H |

4.4.2 TCASE and VCC monitor

In this case, MultiSense output operates in voltage mode and output level is referred to device GND. Care must be taken in case a GND network protection is used, because a voltage shift is generated between the device GND and the microcontroller input GND reference.

Figure 45: "GND voltage shift" shows the link between $V_{MEASURED}$ and the real V_{SENSE} signal.

Figure 45: GND voltage shift



V_{CC} monitor

Battery monitoring channel provides $V_{SENSE} = V_{CC} / 4$.

Case temperature monitor

Case temperature monitor is capable of providing information about the actual device temperature. Since a diode is used for temperature sensing, the following equation describes the link between temperature and output V_{SENSE} level:

$$V_{SENSE_TC}(T) = V_{SENSE_TC}(T_0) + dV_{SENSE_TC} / dT * (T - T_0)$$

where dV_{SENSE_TC} / dT ~ typically -5.5 mV/K (for temperature range (-40 °C to 150 °C)).

4.4.3 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable that V_{PU} is switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

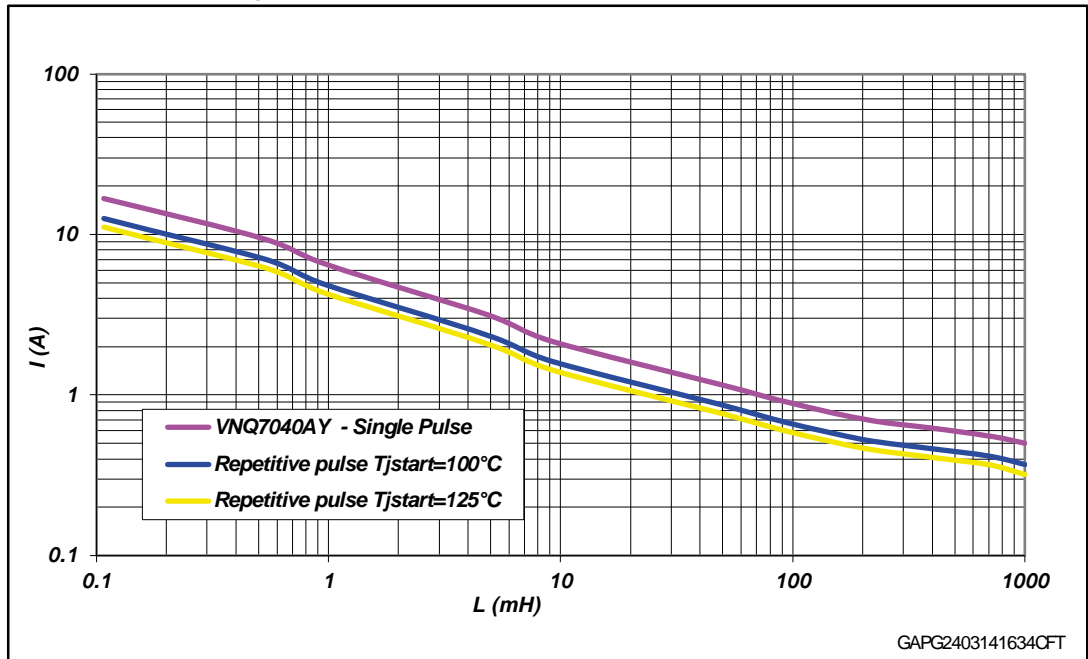
R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

Equation

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off)2min @4V}}$$

5 Maximum demagnetization energy (VCC = 16 V)

Figure 46: Maximum turn off current versus inductance



6 Package and PCB thermal data

6.1 PowerSSO-36 thermal data

Figure 47: PowerSSO-36 PC board

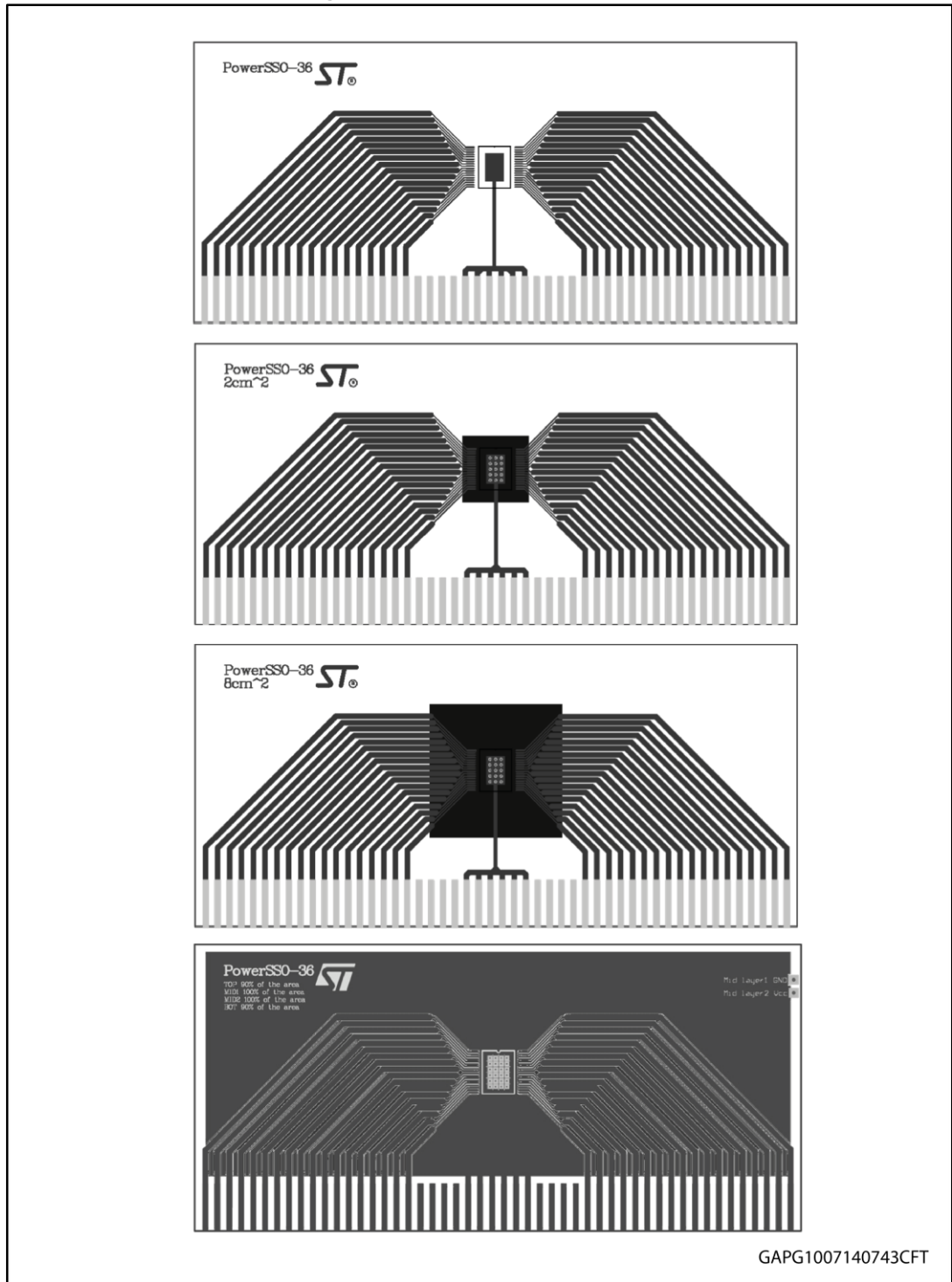


Table 20: PCB properties

| Dimension | Value |
|-----------------------------|--------------------|
| Board finish thickness | 1.6 mm +/- 10% |
| Board dimension | 129 mm x 60 mm |
| Board Material | FR4 |
| Cu thickness (outer layers) | 0.070 mm |
| Cu thickness (inner layers) | 0.035 mm |
| Thermal via separation | 1.2 mm |
| Thermal via diameter | 0.3 mm +/- 0.08 mm |
| Cu thickness on vias | 0.025 mm |
| Footprint dimension | 4.1 mm x 6.5 mm |

Figure 48: Rthj-amb vs PCB copper area in open box free air condition

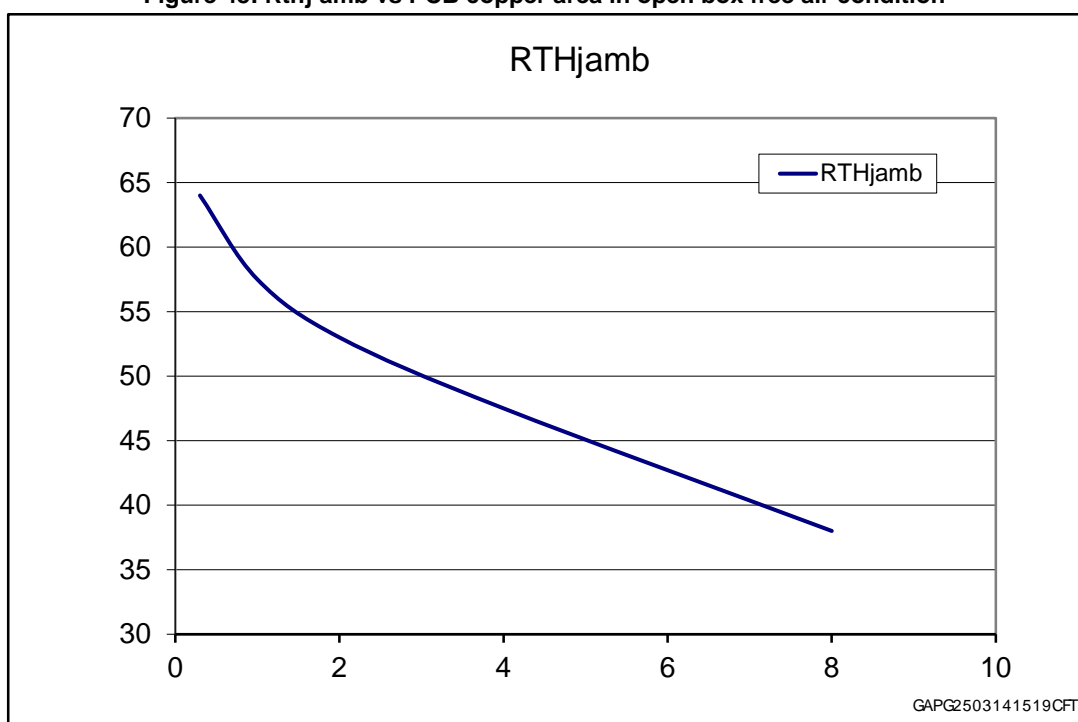


Figure 49: PowerSSO-36 thermal impedance junction ambient

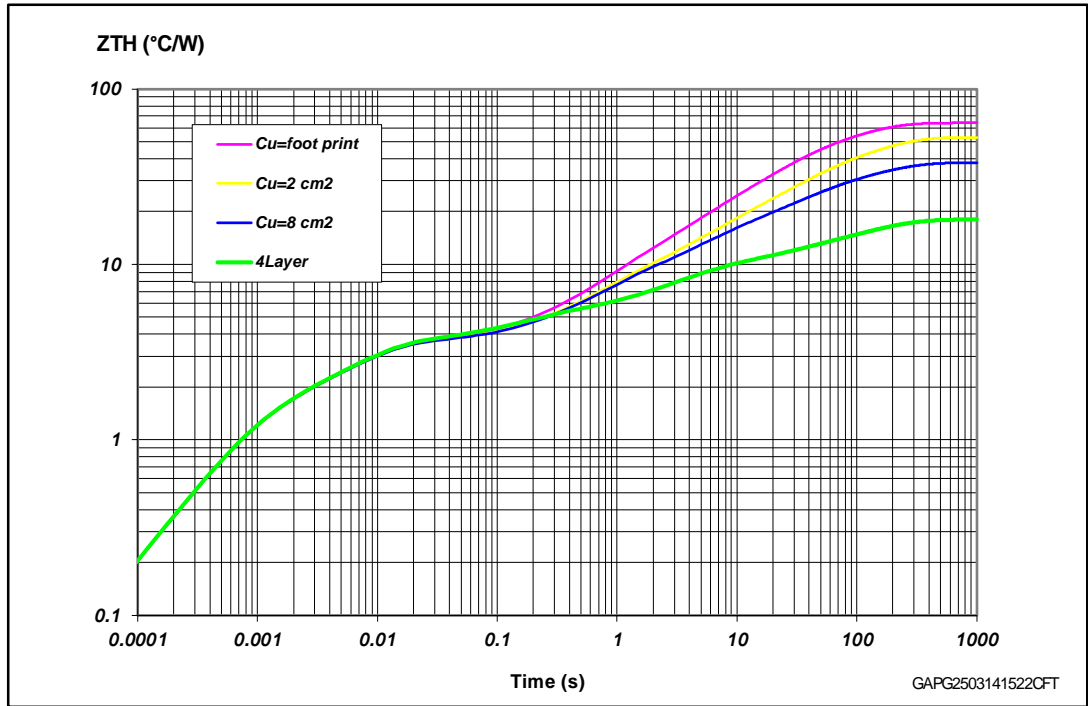


Figure 50: Thermal fitting model of a HSD in PowerSSO-36

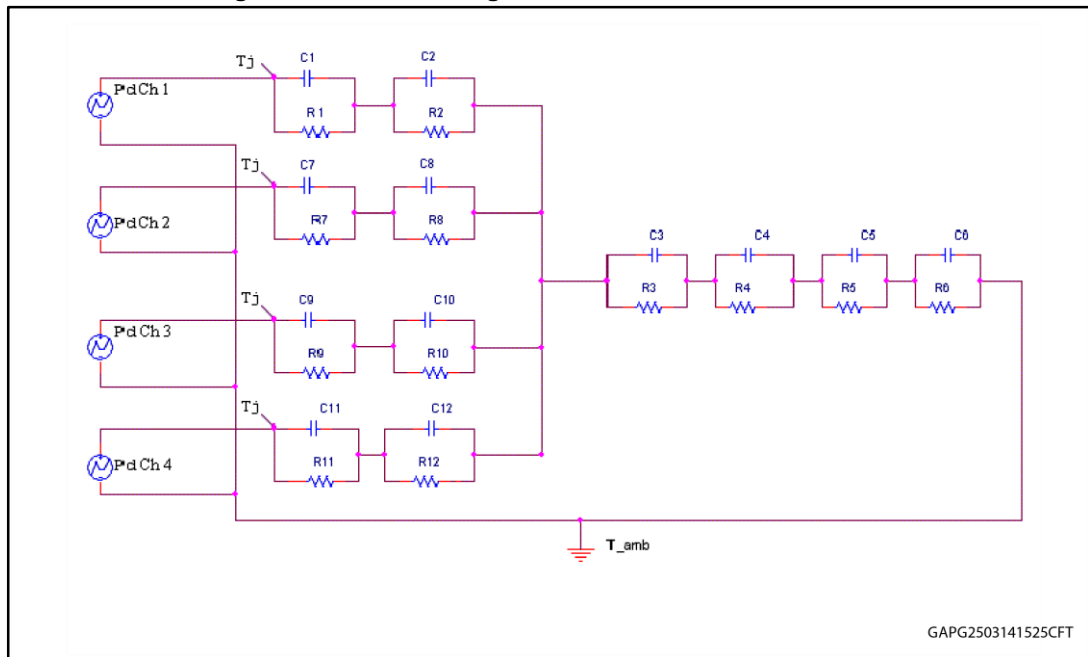


Table 21: Thermal parameters

| Area/island (cm ²) | FP | 2 | 8 | 4L |
|--------------------------------|-----|-----|-----|----|
| R1 = R7 = R9 = R11 (°C/W) | 1.8 | | | |
| R2 = R8 = R10 = R12 (°C/W) | 1.7 | | | |
| R3 (°C/W) | 3.5 | 3.5 | 3.5 | 2 |
| R4 (°C/W) | 8 | 6 | 6 | 4 |

| Area/island (cm ²) | FP | 2 | 8 | 4L |
|--------------------------------|--------|-----|-----|-----|
| R5 (°C/W) | 20 | 14 | 10 | 2 |
| R6 (°C/W) | 30 | 26 | 15 | 7 |
| C1 = C7 = C9 = C11 (W·s/°C) | 0.0005 | | | |
| C2 = C8 = C10 = C12 (W·s/°C) | 0.01 | | | |
| C3 (W·s/°C) | 0.1 | 0.1 | 0.1 | 0.1 |
| C4 (W·s/°C) | 0.5 | 0.8 | 0.8 | 0.8 |
| C5 (W·s/°C) | 1 | 2 | 3 | 10 |
| C6 (W·s/°C) | 3 | 5 | 9 | 18 |

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 PowerSSO-36 package information

Figure 51: PowerSSO-36 package outline

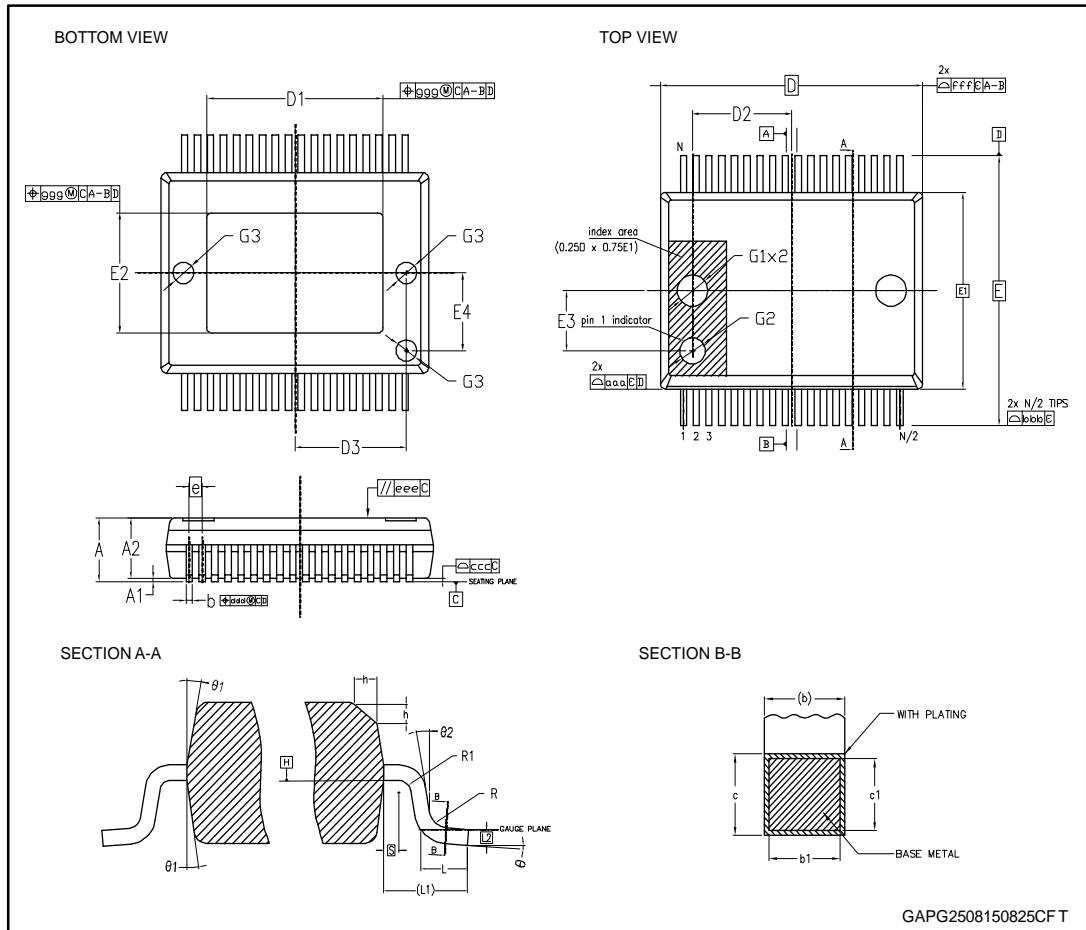


Table 22: PowerSSO-36 mechanical data

| Ref. | Dimensions | | |
|------|-------------|------|------|
| | Millimeters | | |
| | Min. | Typ. | Max. |
| Θ | 0° | | 8° |
| Θ1 | 5° | | 10° |
| Θ2 | 0° | | |
| A | 2.15 | | 2.45 |
| A1 | 0.00 | | 0.10 |

| Ref. | Dimensions | | |
|---------------------------------------|-------------|------|------|
| | Millimeters | | |
| | Min. | Typ. | Max. |
| A2 | 2.15 | | 2.35 |
| b | 0.18 | | 0.32 |
| b1 | 0.13 | 0.25 | 0.30 |
| c | 0.23 | | 0.32 |
| c1 | 0.20 | 0.20 | 0.30 |
| D | 10.30 BSC | | |
| D1 | 6.90 | | 7.50 |
| D2 | | 3.65 | |
| D3 | | 4.30 | |
| e | 0.50 BSC | | |
| E | 10.30 BSC | | |
| E1 | 7.50 BSC | | |
| E2 | 4.30 | | 5.20 |
| E3 | | 2.30 | |
| E4 | | 2.90 | |
| G1 | | 1.20 | |
| G2 | | 1.00 | |
| G3 | | 0.80 | |
| h | 0.30 | | 0.40 |
| L | 0.55 | 0.70 | 0.85 |
| L1 | 1.40 REF | | |
| L2 | 0.25 BSC | | |
| N | 36 | | |
| R | 0.30 | | |
| R1 | 0.20 | | |
| S | 0.25 | | |
| Tolerance of form and position | | | |
| aaa | 0.20 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.20 | | |
| eee | 0.10 | | |
| fff | 0.20 | | |
| ggg | 0.15 | | |

7.2 PowerSSO-36 packing information

Figure 52: PowerSSO-36 reel 13"

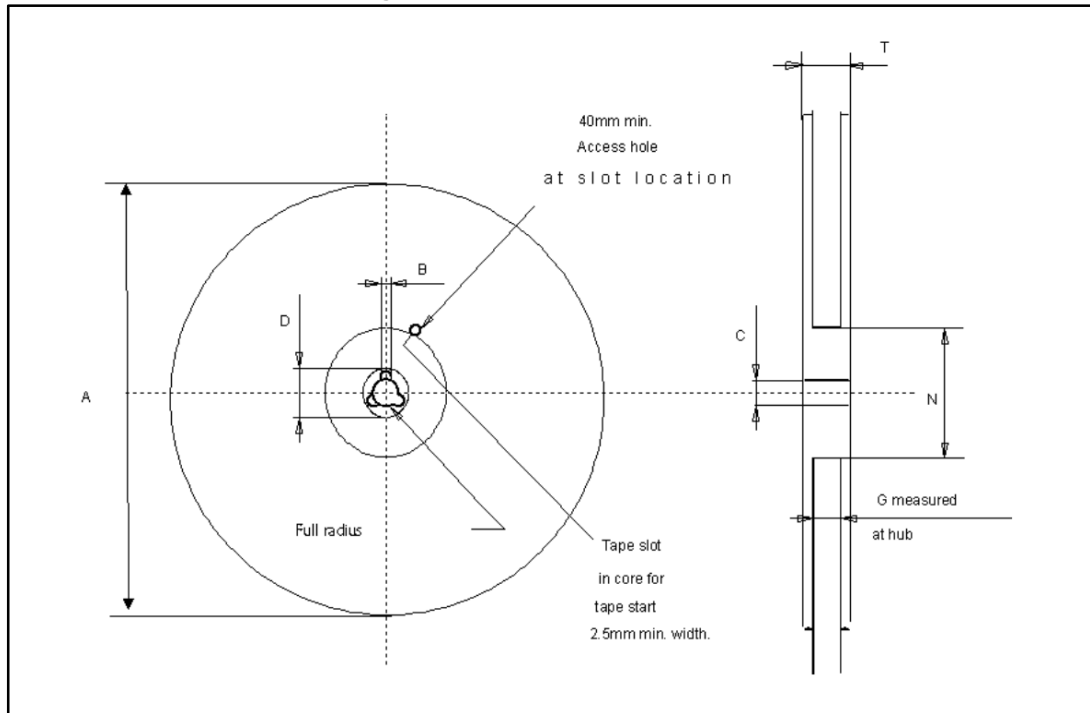


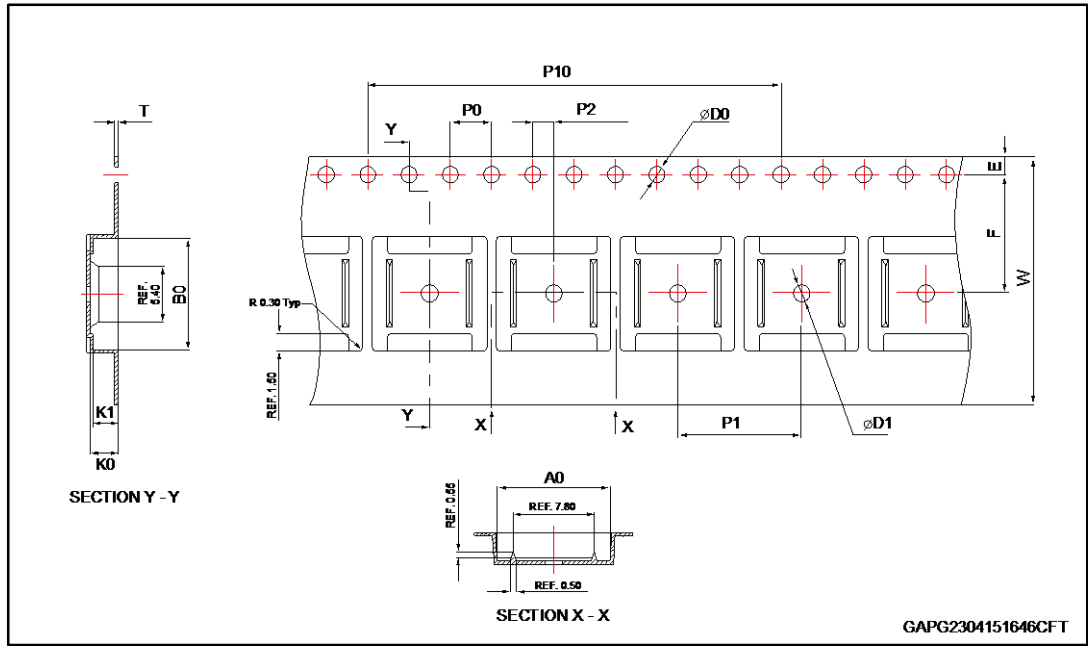
Table 23: Reel dimensions

| Description | Value ⁽¹⁾ |
|-----------------|----------------------|
| Base quantity | 1000 |
| Bulk quantity | 1000 |
| A (max) | 330 |
| B (min) | 1.5 |
| C (± 0.2) | 13 |
| F | 20.2 |
| G (+2 / -0) | 24.4 |
| N (min) | 100 |
| T (max) | 30.4 |

Notes:

⁽¹⁾All dimensions are in mm.

Figure 53: PowerSSO-36 carrier tape



GAPG2304151646CFT

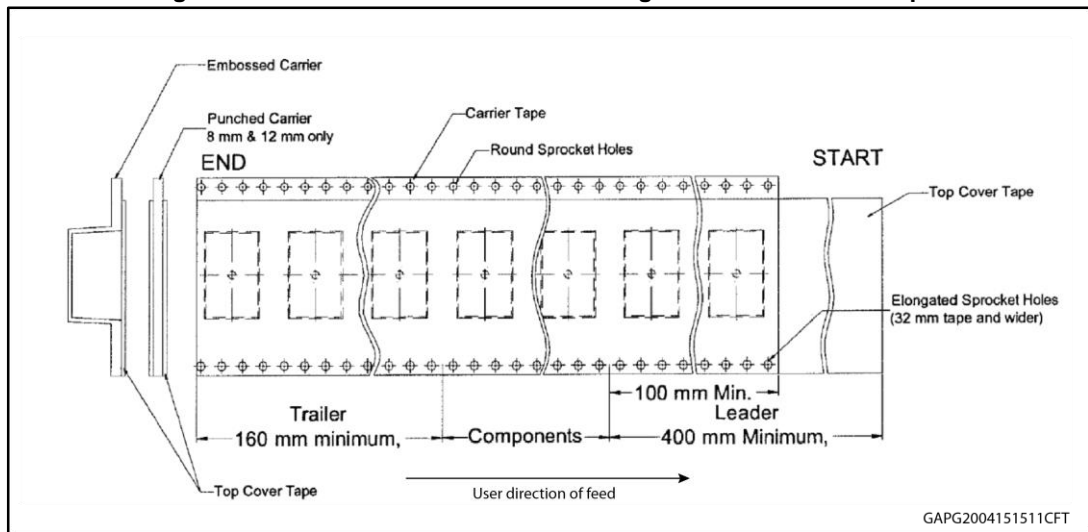
Table 24: PowerSSO-36 carrier tape dimensions

| Description | Value ⁽¹⁾ |
|-----------------|----------------------|
| A ₀ | 10.90 ± 0.10 |
| B ₀ | 10.80 ± 0.10 |
| K ₀ | 2.75 ± 0.10 |
| K ₁ | 2.45 ± 0.10 |
| D ₀ | 1.50 (+0.10 / -0) |
| D ₁ | 1.60 ± 0.10 |
| P ₀ | 4.00 ± 0.10 |
| P ₁ | 12.00 ± 0.10 |
| P ₂ | 2.00 ± 0.10 |
| P ₁₀ | 40.00 ± 0.20 |
| E | 1.75 ± 0.10 |
| F | 11.50 ± 0.10 |
| W | 24.00 ± 0.30 |
| T | 0.30 ± 0.05 |

Notes:

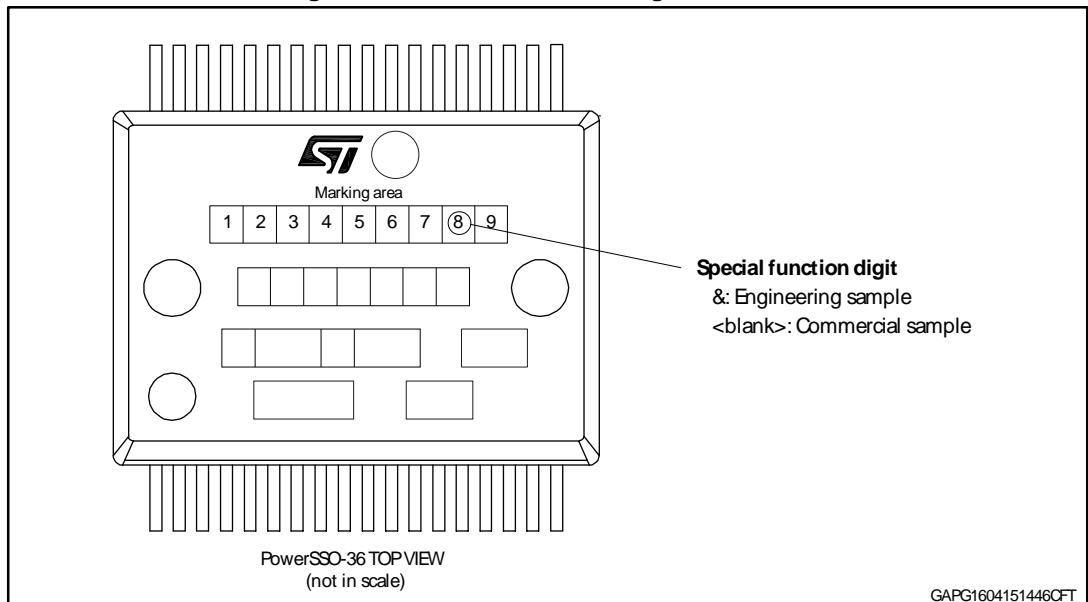
⁽¹⁾All dimensions are in mm.

Figure 54: PowerSSO-36 schematic drawing of leader and trailer tape



7.3 PowerSSO-36 marking information

Figure 55: PowerSSO-36 marking information



Engineering Samples: Parts marked as & are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

8 Order codes

Table 25: Device summary

| Package | Order codes |
|-------------|---------------|
| | Tape and reel |
| PowerSSO-36 | VNQ7040AYTR |

9 Revision history

Table 26: Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 21-Oct-2015 | 1 | Initial release. |
| 02-May-2016 | 2 | Added "AEC-Q100 qualified" in Features Upated Table 4: "Thermal data" Upated Table 8: "MultiSense" Updated Section 6: "Package and PCB thermal data" |
| 15-Jul-2016 | 3 | Updated Figure 52: "PowerSSO-36 reel 13" and Table 23: "Reel dimensions" |

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved