NCV894530

1.2 A - 2.1 MHz High Efficiency Low Voltage Step-Down Converter

The NCV894530 step−down dc−dc converter is a monolithic integrated circuit dedicated to automotive driver information systems from a downstream voltage rail. The output voltage is externally adjustable from 0.9 V to 3.3 V and can source up to 1.2 A. The converter is running at a 2.1 MHz switching frequency, above the sensitive AM band. The NCV894530 provides additional features expected in automotive power systems such as integrated soft−start, hiccup mode current limit and thermal shutdown protection. The device can also be synchronized to an external clock signal in the range of 2.1 MHz. The NCV894530 is available in the same 3x3 mm 10−pin DFN package as the dual NCV896530, with compatible pin−out.

Features

- Synchronous Rectification for Higher Efficiency
- 2.1 MHz Switching Frequency
- Sources up to 1.2 A
- Adjustable Output Voltage from 0.9 V to 3.3 V
- 2.7 V to 5.5 V Input Voltage Range
- Thermal Limit and Short Circuit Protection
- Auto Synchronizes with an External Clock
- Wettable Flanks − DFN
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Audio
- Infotainment
- Safety − Vision System
- Instrumentation

ON Semiconductor®

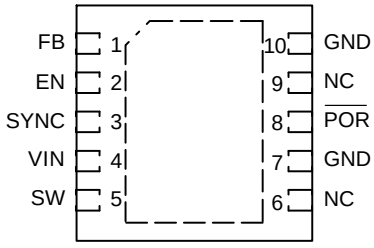
www.onsemi.com

DFN10
CASE 485C

MARKING DIAGRAM

NCV89
4530 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCV894530MWTXG	DFN10 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

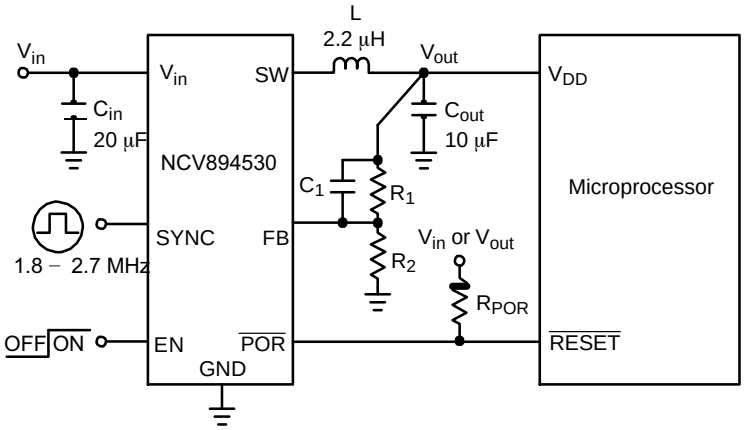


Figure 1. NCV894530 Typical Application

BLOCK DIAGRAM

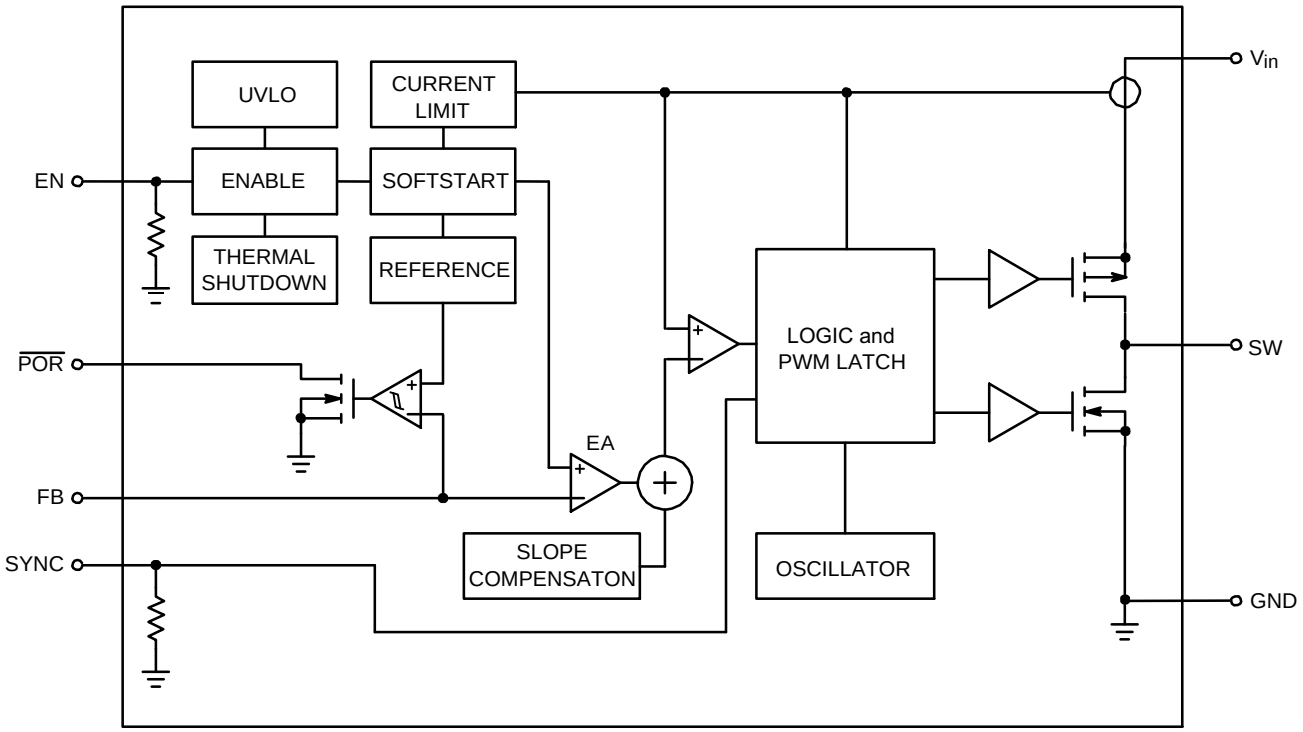


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
1	FB	Analog Input	Feedback voltage. This is the input to the error amplifier.
2	EN	Digital Input	Enable. This pin is active HIGH (equal or lower Analog Input voltage) and is turned off by logic LOW. Do not let this pin float.
3	SYNC	Digital Input	Oscillator Synchronization. This pin can be synchronized to an external clock in the range of 2.1 MHz. If not used, the pin must be connected to ground.
4	VIN	Analog / Power Input	Power supply input for the PFET power stage, analog and digital blocks. The pin must be decoupled to ground by a 10 μF ceramic capacitor.
5	SW	Power Output	Connection from power MOSFETs of output to the Inductor.

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
6	NC	−	
7	GND	Analog / Power Ground	This pin is the GROUND reference for the analog section of the IC. The pin must be connected to the system ground. Both pins must be connected together on PCB.
8	$\overline{POR}$	Digital Output	Power On Reset. This is an open drain output. This output is shutting down when the output voltage is less than 90% (typ) of their nominal values. An external pull−up resistor should be connected between POR and V_{IN} or V_{OUT} depending on the supplied device.
9	NC	−	
10	GND	Analog Ground	Connect this pin to ground.
EPAD	EPAD	Exposed Pad	Connected to GND potential.

ABSOLUTE MAXIMUM RATINGS

(Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.)

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{in}	−0.3	6.0	V
SW Voltage	V_{SW}	−0.3	6 V (or V_{in} + 0.3 V)*	V
Enable Input Voltage	V_{EN}	−0.3	6 V (or V_{in} + 0.3 V)*	V
Feedback Input Voltage	V_{FB}	−0.3	6 V (or V_{in} + 0.3 V)*	V
Oscillator Synchronization Input Voltage	V_{SYNC}	−0.3	6 V (or V_{in} + 0.3 V)*	V
Power On Reset Voltage	V_{POR}	−0.3	6 V (or V_{in} + 0.3 V)*	V
Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Whichever is lower.

ESD CAPABILITY (Note 1)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESDHBM	−2	2	kV
ESD Capability, Machine Model	ESDMM	−200	200	V

1. This device series incorporates ESD portection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)

LEAD SOLDERING TEMPERATURE AND MSL (Note 2)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL	3		per IPC
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions	T_{SLD}		265 peak	°C

2. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, DFN10 (Note 3) Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	40	°C/W

3. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

ELECTRICAL CHARACTERISTICS

(2.7 V < V_{IN} < 5.5 V, Min and Max values are valid for the temperature range −40°C ≤ T_J ≤ +150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_A = +25°C)

Rating	Conditions	Symbol	Min	Typ	Max	Unit
INPUT VOLTAGE						
Quiescent Current	SYNC = GND, V_{FB} = 0 V, EN = 2 V, (No Switching)	I_q	−	1.0	2.0	mA
Shutdown Current	EN = 0 V	I_{OFF}	−	−	10	μA
Under Voltage Lockout	V_{IN} falling	V_{UVLO}	2.2	2.4	2.6	V
Under Voltage Hysteresis		V_{UVLOH}	−	100	150	mV
SYNC						
SYNC Threshold Voltage Logic Low Logic High		 V_{ILSYNC} V_{IHSYNC}	 − 1.2	 − −	 0.4 −	V
SYNC Input Current	V_{SYNC} = 5 V	I_{SYNC}	2.0	−	50	μA
External Synchronization		f_{SYNC}	1.8	−	2.7	MHz
SYNC Pulse Duty Ratio		D_{SYNC}	−	50	−	%
ENABLE						
Enable Threshold Voltage Logic Low Logic High		 V_{ILEN} V_{IHEN}	 − 1.2	 − −	 0.4 −	V
Enable Input Current	V_{EN} = 5 V	I_{EN}	2	−	50	μA
POWER ON RESET						
Power On Reset Threshold	V_{OUT} falling	V_{PORT}	87	90	93	%Vout
Power On Reset Hysteresis		V_{PORH}	−	−	3.0	%Vout
POR Sink Current	V_{POR} = 0.4 V	I_{POR}	2.0	−	−	mA
FEEDBACK VOLTAGE						
Feedback Voltage (Accuracy %)	T_J = −40°C to 125°C	V_{FB}	0.591 (−1.5%)	0.6	0.609 (+1.5%)	V
Soft−Start Time	Time from EN to 90% of V_{FB}	t_{SS}	1700	−	3200	μs
SWITCHING FREQUENCY						
Switching Frequency		F_{SW}	1.8	2.1	2.4	MHz
Duty Cycle		D	−	−	100	%
Minimum On Time		T_{ONmin}	−	−	80	ns
POWER SWITCHES						
High−Side MOSFET On−Resistance	$I_{RDS(on)}$ = 0.6 A, V_{IN} = 5 V, T_J = 25°C	$R_{DS(on)H}$	−	500	820	mΩ
Low−Side MOSFET On−Resistance	$I_{RDS(on)}$ = 0.6 A, V_{IN} = 5 V, T_J = 25°C	$R_{DS(on)L}$	−	450	820	mΩ
High−Side MOSFET Leakage Current	V_{IN} = 5 V, V_{SW} = 0 V, V_{EN} = 0 V	$I_{DS(off)H}$	−	−	5.0	μA
Low−Side MOSFET Leakage Current	V_{SW} = 5 V, V_{EN} = 0 V	$I_{DS(off)L}$	−	−	5.0	μA
CURRENT LIMIT PROTECTION						
Current Limit	Peak Inductor Current (100% duty cycle)	I_{PK}	1.9	−	2.5	A
THERMAL SHUTDOWN						
Thermal Shutdown Temperature	Guaranteed by Design	T_{SD}	150	170	190	°C
Thermal Shutdown Hysteresis	Guaranteed by Design	T_{SH}	5.0	−	20	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS CURVES

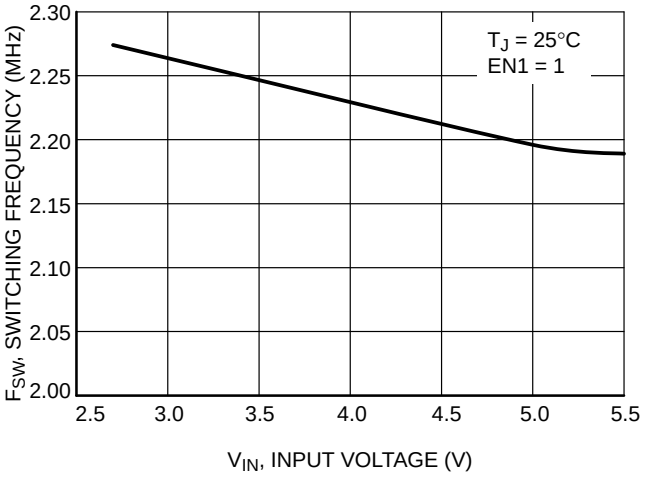


Figure 3. Switching Frequency vs. Input Voltage

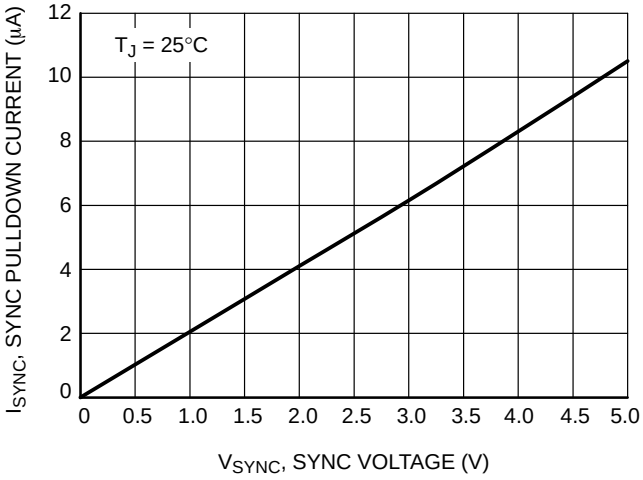


Figure 4. Sync Pulldown Current vs. Sync Voltage

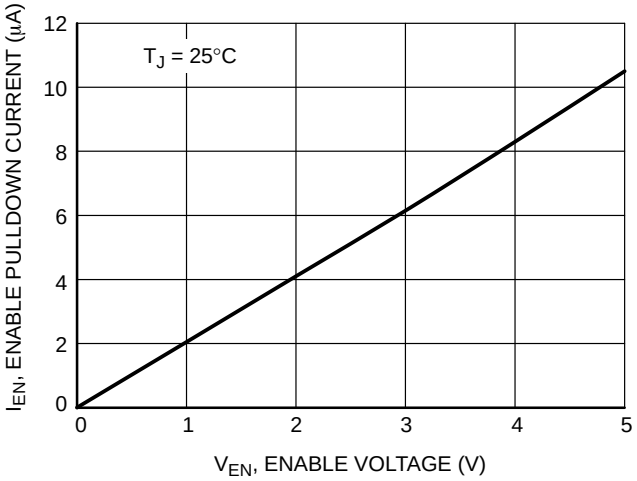


Figure 5. Enable Pulldown Current vs. Enable Voltage

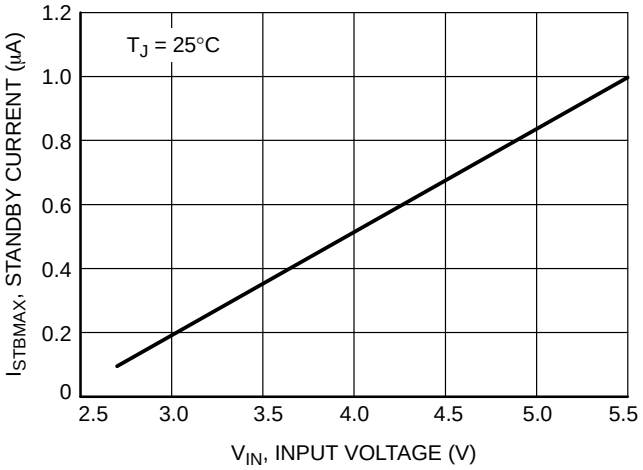


Figure 6. Standby Current vs. Input Voltage

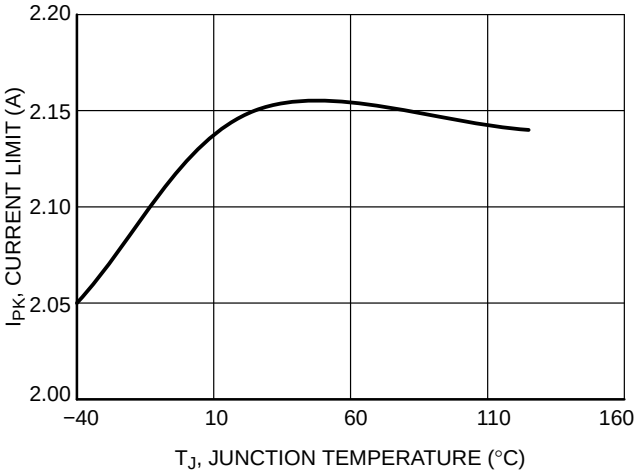


Figure 7. Current Limit vs. Temperature

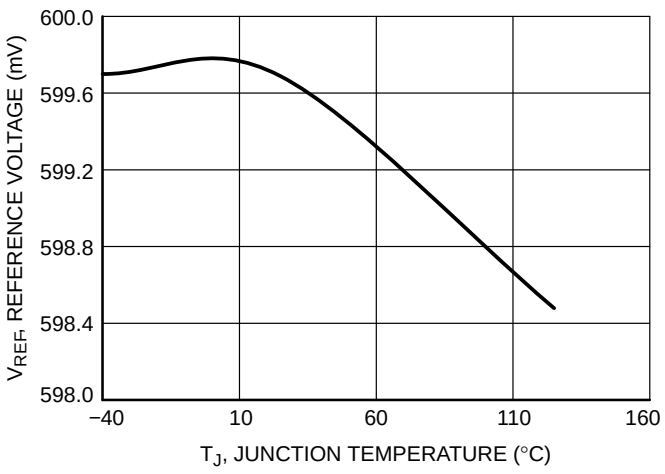


Figure 8. Reference Voltage vs. Temperature

TYPICAL CHARACTERISTICS CURVES

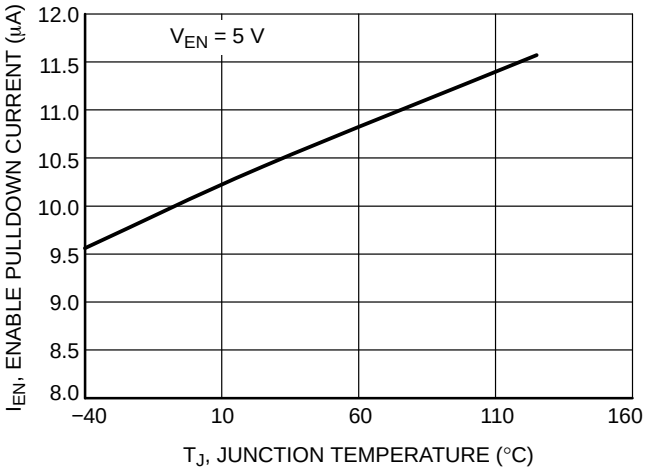


Figure 9. Enable Pulldown Current vs. Temperature

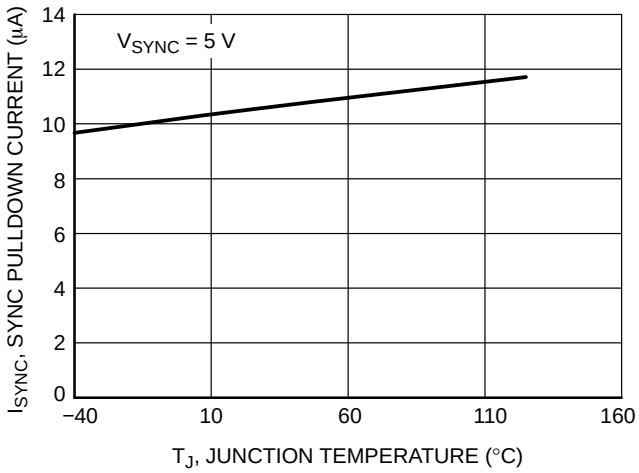


Figure 10. Sync Pulldown Current vs. Temperature

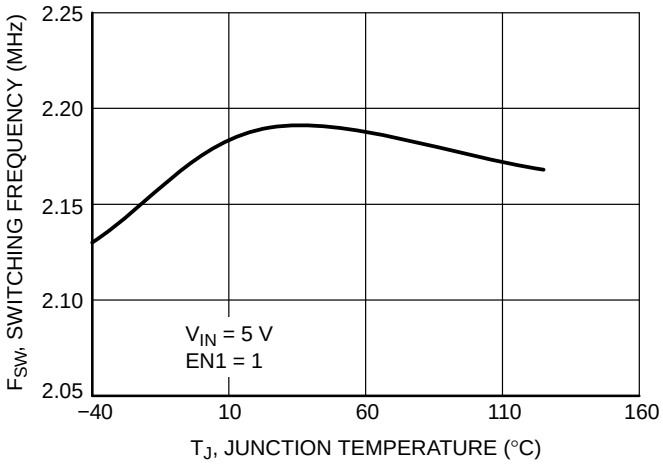


Figure 11. Switching Frequency vs. Temperature

APPLICATION INFORMATION

PWM Operating Mode

The output voltage of the device is regulated by modulating the on−time pulse width of the main switch PMOS at a fixed 2.1 MHz frequency (Figure 2).

The switching of the PMOS is controlled by a flip−flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the sum of the sensed current signal and compensation ramp.

The driver switches ON and OFF the upper side transistor and switches the lower side transistor in either ON state or in current source mode.

At the beginning of each cycle, the main switch is turned ON by the rising edge of the internal oscillator clock. The inductor current ramps up until the sum of the current sense signal and compensation ramp becomes higher than the error amplifier's voltage. Once this has occurred, the PWM comparator resets the flip−flop, PMOS is turned OFF while the synchronous switch NMOS is turned in its current source mode. NMOS replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure PMOS is completely turned OFF before NMOS is being turned ON.

Soft−Start

The NCV894530 uses soft start to limit the inrush current when the device is initially powered up or enabled. Soft−start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft−start capacitor to provide gradually increasing reference voltage. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage.

Over Current Hiccup Protection

When the current through the inductor exceeds the current limit the NCV894530 enters over current hiccup mode. When an over current event is detected the NCV894530 disables the outputs and attempts to re−enable the outputs after the hiccup time. The part remains off for the hiccup time and then goes through the power on reset procedure. If the excessive load has been removed then the output stage re−enables and operates normally; however, if the excessive load is still present the cycle begins again. Internal heat dissipation is kept to a minimum as current will only flow during the reset time of the protection circuitry. The hiccup mode is continuous until the excessive load is removed. The hiccup current limit in switching mode is 300 mA lower than it in low dropout mode (100% duty cycle).

Low Dropout Operation

The NCV894530 offers a low input−to−output voltage difference. The NCV894530 can operate at 100% duty cycle.

In this mode the PMOS remains completely ON. The minimum input voltage to maintain regulation can be calculated as:

$$V_{IN(min)} = V_{OUT(max)} + \left(I_{OUT} \left(R_{DS(on)} + R_{INDUCTOR} \right) \right) \quad \text{(eq. 1)}$$

V_{OUT}: Output Voltage
I_{OUT}: Max Output Current
$R_{DS(on)}$: P=Channel Switch $R_{DS(on)}$
$R_{INDUCTOR}$: Inductor Resistance (DCR)

Power On Reset

The Power On Reset (POR) is pulled low when the converter is out of 90% of the regulation. When output is in the range of regulation, a pull−up resistor is needed to this open drain output. This resistor may be connected to VIN or VOUT if the device supplied cannot accept VIN on the IO pins. POR is low when NCV894530 is off. Leave the POR pin unconnected when not used.

Frequency Synchronization

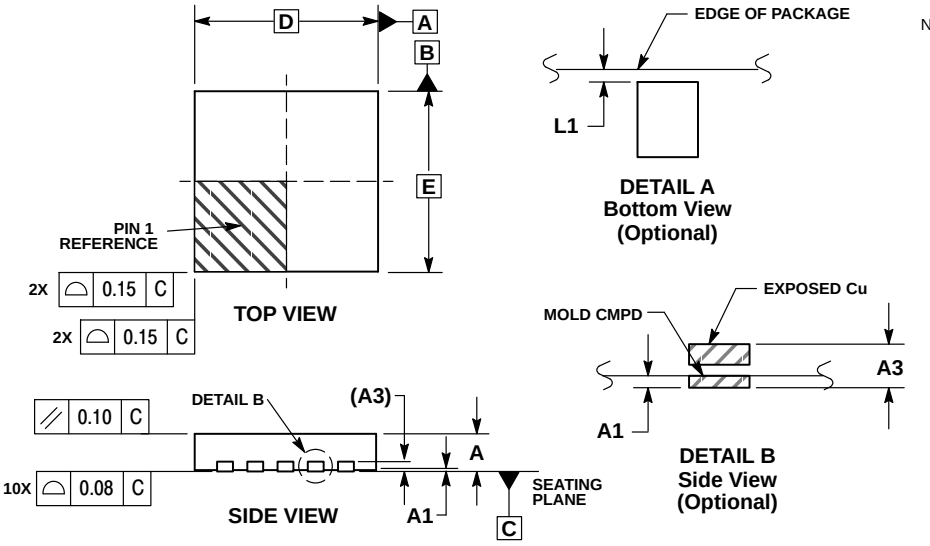
The NCV894530 can be synchronized with an external clock signal by the SYNC pin (1.8 MHz − 2.7 MHz).

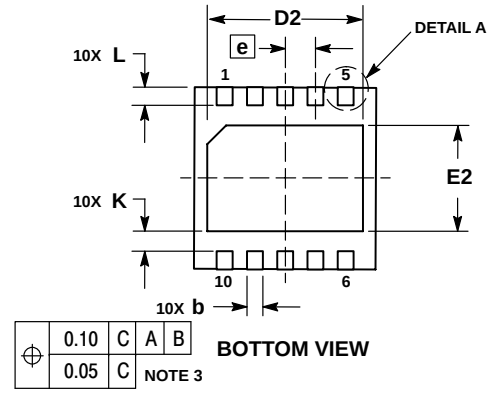
Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. If the junction temperature exceeds TSD, the device shuts down. In this mode all power transistors and control circuits are turned off. The device restarts in soft−start after the temperature drops below 130°C min. This feature is provided to prevent catastrophic failures from accidental device overheating.

PACKAGE DIMENSIONS

DFN10, 3x3, 0.5P
CASE 485C
ISSUE C

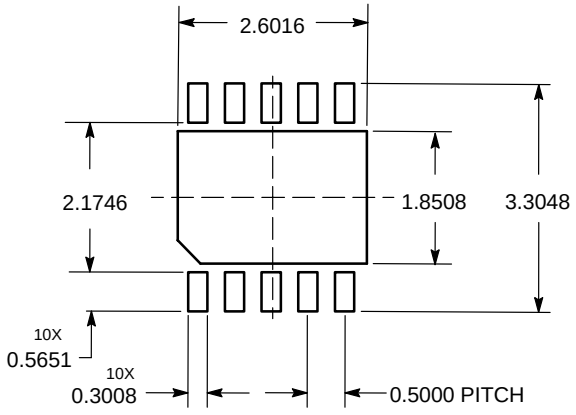




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASHING MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL b.
6. DETAILS A AND B SHOW OPTIONAL VIEWS FOR END OF TERMINAL LEAD AT EDGE OF PACKAGE.
7. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	2.40	2.60
E	3.00 BSC	
E2	1.70	1.90
e	0.50 BSC	
K	0.19 TYP	
L	0.35	0.45
L1	0.00	0.03

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative