

CBTW28DD14

14-bit bus switch/multiplexer for DDR2-DDR3 applications

Rev. 2 — 26 July 2012

Product data sheet

1. General description

This 14-bit bus switch/multiplexer (MUX) is designed for 1.5 V or 1.8 V supply voltage operation, SSTL_15 or SSTL_18 signaling and CMOS select input levels. It is designed for operation in DDR2 or DDR3 memory bus systems, with speeds up to 1600 MT/s.

The CBTW28DD14 has a 1 : 2 switch or 2 : 1 multiplex topology and offers a 14-bit wide bus. Each 14-bit wide A-port can be switched to one of two ports B and C, for all bits simultaneously. The selection of the port is by a simple CMOS input (SElect). Another CMOS input (ENable) is available to allow all ports to be disconnected. Each port is non-directional due to the use of FET switches, allowing a multitude of applications requiring high-bandwidth switching or multiplexing.

The device is able to operate transparently in 1.5 V as well as 1.8 V applications. Typical usage is SSTL_15 signaling when using a supply voltage of 1.5 V, and SSTL_18 signaling when using a supply voltage of 1.8 V. The SEL and EN input signals are designed to operate transparently as CMOS input level signals in both 1.5 V and 1.8 V supply voltage conditions.

CBTW28DD14 uses NXP's proprietary high-speed switch architecture providing high bandwidth, very little insertion loss at low frequency, and very low propagation delay, allowing use in many applications requiring switching or multiplexing of high-speed signals. It is available in a 4.5 mm × 4.5 mm TFBGA48 package with 0.5 mm ball pitch, for optimal size versus board layout density considerations. It is characterized for operation from -10 °C to +85 °C.

2. Features and benefits

2.1 Topology

- 14-bit bus width
- 1 : 2 switch/MUX topology
- Bidirectional operation
- Simple CMOS select pin (SEL)
- Simple CMOS enable pin (EN)

2.2 Performance

- 1600 MT/s throughput
- 2.5 GHz bandwidth
- Low ON insertion loss
- Low crosstalk
- High OFF isolation



- SSTL_15 or SSTL_18 signaling
- Low R_{ON} (10 Ω typical)

2.3 General attributes

- 1.5 V or 1.8 V supply voltage operation
- Very low supply current (300 μA typical)
- ESD robustness exceeds 3 kV HBM, 1 kV CDM
- Available in TFBGA48 package, 4.5 mm × 4.5 mm × 0.8 mm size, 0.5 mm pitch, Pb-free/Dark Green

3. Applications

- DDR2 memory bus systems
- DDR3 memory bus systems
- Systems requiring high-speed multiplexing

4. Ordering information

Table 1. Ordering information

| Type number | Topside mark | Package | | Version |
|--------------|--------------|---------|--|-----------|
| | | Name | Description | |
| CBTW28DD14ET | W2814 | TFBGA48 | plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.8 mm | SOT1155-1 |

5. Functional diagram

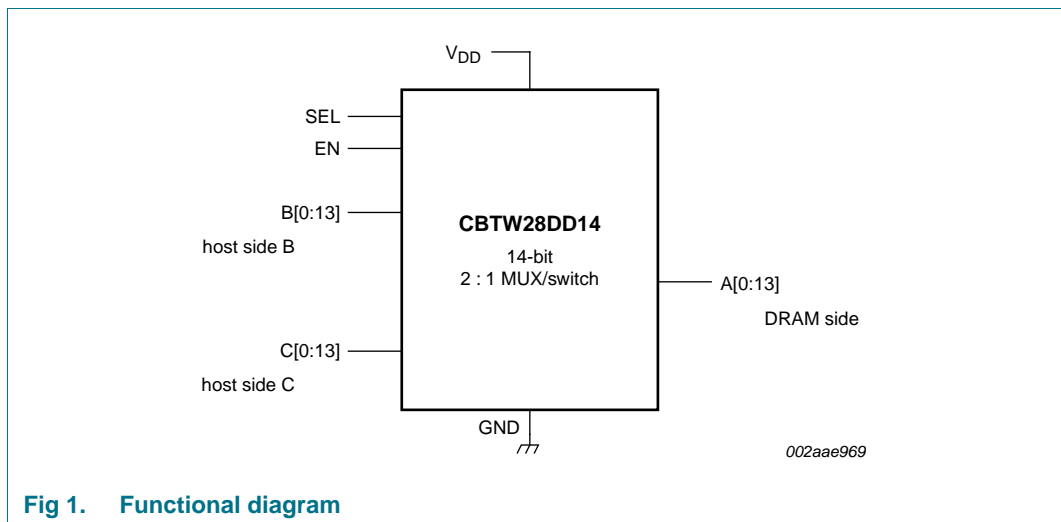
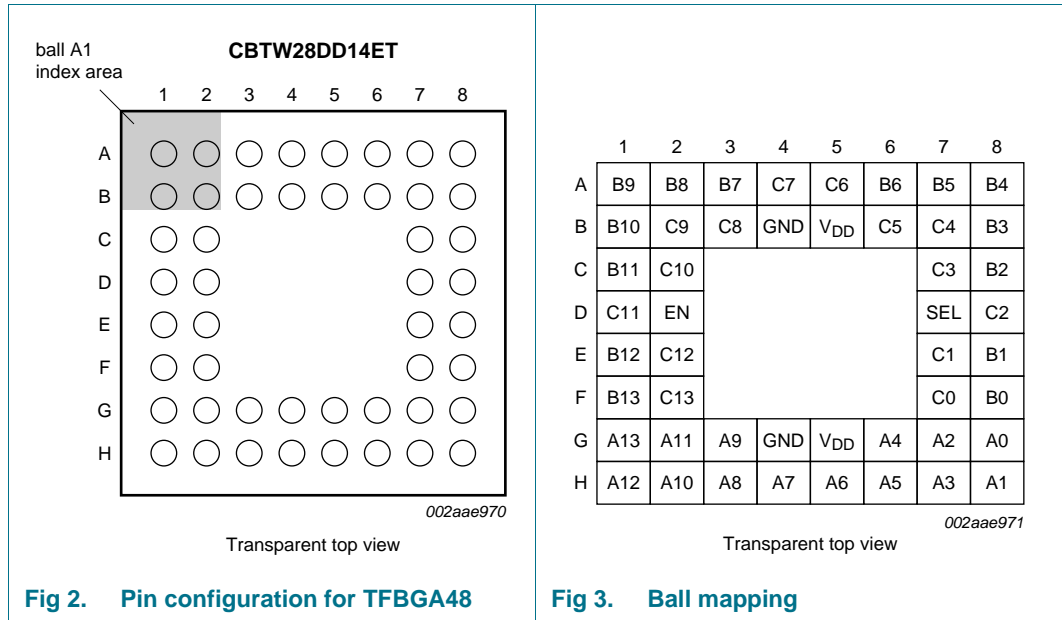


Fig 1. Functional diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Type | Description |
|-----------------|--|----------------|---|
| A[0:13] | G8, H8, G7, H7, G6, H6, H5, H4, H3, G3, H2, G2, H1, G1 | high-speed I/O | 14-bit wide input/output, port A |
| B[0:13] | F8, E8, C8, B8, A8, A7, A6, A3, A2, A1, B1, C1, E1, F1 | high-speed I/O | 14-bit wide input/output, port B |
| C[0:13] | F7, E7, D8, C7, B7, B6, A5, A4, B3, B2, C2, D1, E2, F2 | high-speed I/O | 14-bit wide input/output, port C |
| SEL | D7 | CMOS input | CMOS input signal. When SEL = LOW, port A and port B are mutually connected. When SEL = HIGH, port A and port C are mutually connected. |
| EN | D2 | CMOS input | CMOS input signal. When LOW, all ports are mutually isolated. When HIGH, connection is set using the SEL input signal. |
| V _{DD} | B5, G5 | supply | supply voltage connection |
| GND | B4, G4 | ground | ground connection |

7. Functional description

Refer to [Figure 1 “Functional diagram”](#).

The CBTW28DD14 uses a 1.5 V or 1.8 V power supply. All signal paths are implemented using high-bandwidth pass-gate technology and are non-directional. No clock or reset signal is needed for the multiplexer to function. The switch position for the channels is selected using the select signal SEL. The detailed operation is described in [Section 7.1](#).

7.1 Function selection

The internal multiplexer switch position is controlled by two logic inputs, SEL and EN, as described in [Table 3](#).

When a channel is not being used, Port B and Port C of this channel should be tied to ground. For example, if Channel 2 is not used, B2 and C2 should be tied to ground and A2 should be left open.

Table 3. Function selection

X = don't care.

| Inputs | | Switch position | |
|--------|------|-----------------|-----------------|
| EN | SEL | A ↔ B | A ↔ C |
| LOW | X | OFF (isolating) | OFF (isolating) |
| HIGH | LOW | ON (conducting) | OFF (isolating) |
| HIGH | HIGH | OFF (isolating) | ON (conducting) |

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------|---------------------------------|------------------------------------|-------|------|------|
| V _{DD} | supply voltage | | -0.3 | +2.5 | V |
| T _{case} | case temperature | for operation within specification | -40 | +85 | °C |
| V _{ESD} | electrostatic discharge voltage | HBM | [1] - | 3000 | V |
| | | CDM | [2] - | 1000 | V |

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing. Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged-Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged-Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

9. Recommended operating conditions

Table 5. Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---------------------|-----------------------|------|------------|----------------|------|
| V_{DD} | supply voltage | | 1.4 | 1.5 or 1.8 | 2.0 | V |
| V_I | input voltage | all inputs | -0.3 | - | $V_{DD} + 0.3$ | V |
| T_{amb} | ambient temperature | operating in free air | -10 | - | +85 | °C |

10. Static characteristics

Table 6. Static characteristics

$V_{DD} = 1.4\text{ V to }2.0\text{ V}$; $T_{amb} = -10\text{ °C to }+85\text{ °C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|----------|--------------------------|---|-------------|--------------------|-------------|------|
| I_{DD} | supply current | EN = HIGH; $V_{DD} = 1.8\text{ V}$ | - | 0.3 | 1 | mA |
| | | EN = LOW; $V_{DD} = 1.8\text{ V}$ | - | - | 10 | μA |
| I_{IH} | HIGH-level input current | $V_{DD} = 2.0\text{ V}$; $V_I = V_{DD}$ | - | - | ±5 | μA |
| I_{IL} | LOW-level input current | $V_{DD} = 2.0\text{ V}$; $V_I = \text{GND}$ | - | - | ±5 | μA |
| V_{IH} | HIGH-level input voltage | SEL, EN pins | $0.8V_{DD}$ | - | - | V |
| V_{IL} | LOW-level input voltage | SEL, EN pins | -0.5 | - | $0.2V_{DD}$ | V |
| V_{IK} | input clamping voltage | $V_{DD} = 2.0\text{ V}$; $I_I = -18\text{ mA}$ | - | -0.7 | -1.2 | V |

[1] Typical values are at $V_{DD} = 1.8\text{ V}$, $T_{amb} = 25\text{ °C}$, and maximum loading.

11. Dynamic characteristics

Table 7. Dynamic characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|-----------------------|--|------|------|----------------|------|
| $t_{startup}$ | start-up time | supply voltage valid or EN going HIGH to channel specified operating characteristics | - | - | 1 | ms |
| t_{rcfg} | reconfiguration time | SEL state change to channel specified operating characteristics | - | - | 1 | ms |
| V_I | input voltage | | -0.3 | - | $V_{DD} + 0.3$ | V |
| $V_{bias(DC)}$ | bias voltage (DC) | | 0 | - | 2.0 | V |
| α_{il} | insertion loss | channel is on; $0\text{ Hz} \leq f \leq 1.0\text{ GHz}$ | -2.5 | -1.5 | - | dB |
| | | channel is on; $f = 2.5\text{ GHz}$ | -4.5 | - | - | dB |
| | | channel is off; $0\text{ Hz} \leq f \leq 3.0\text{ GHz}$ | - | - | -20 | dB |
| RL_{in} | input return loss | channel is on; $0\text{ Hz} \leq f \leq 1.0\text{ GHz}$ | - | - | -10 | dB |
| α_{ct} | crosstalk attenuation | adjacent channels are on; $0\text{ Hz} \leq f \leq 1.0\text{ GHz}$ | - | - | -25 | dB |
| B | bandwidth | -3.0 dB intercept | - | 2.5 | - | GHz |
| t_{PD} | propagation delay | from A port to B port or C port or vice versa | - | 80 | - | ps |
| t_{sk} | skew time | from any output to any output | - | - | 20 | ps |

12. Package outline

TFBGA48: plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 x 4.5 x 0.8 mm

SOT1155-1

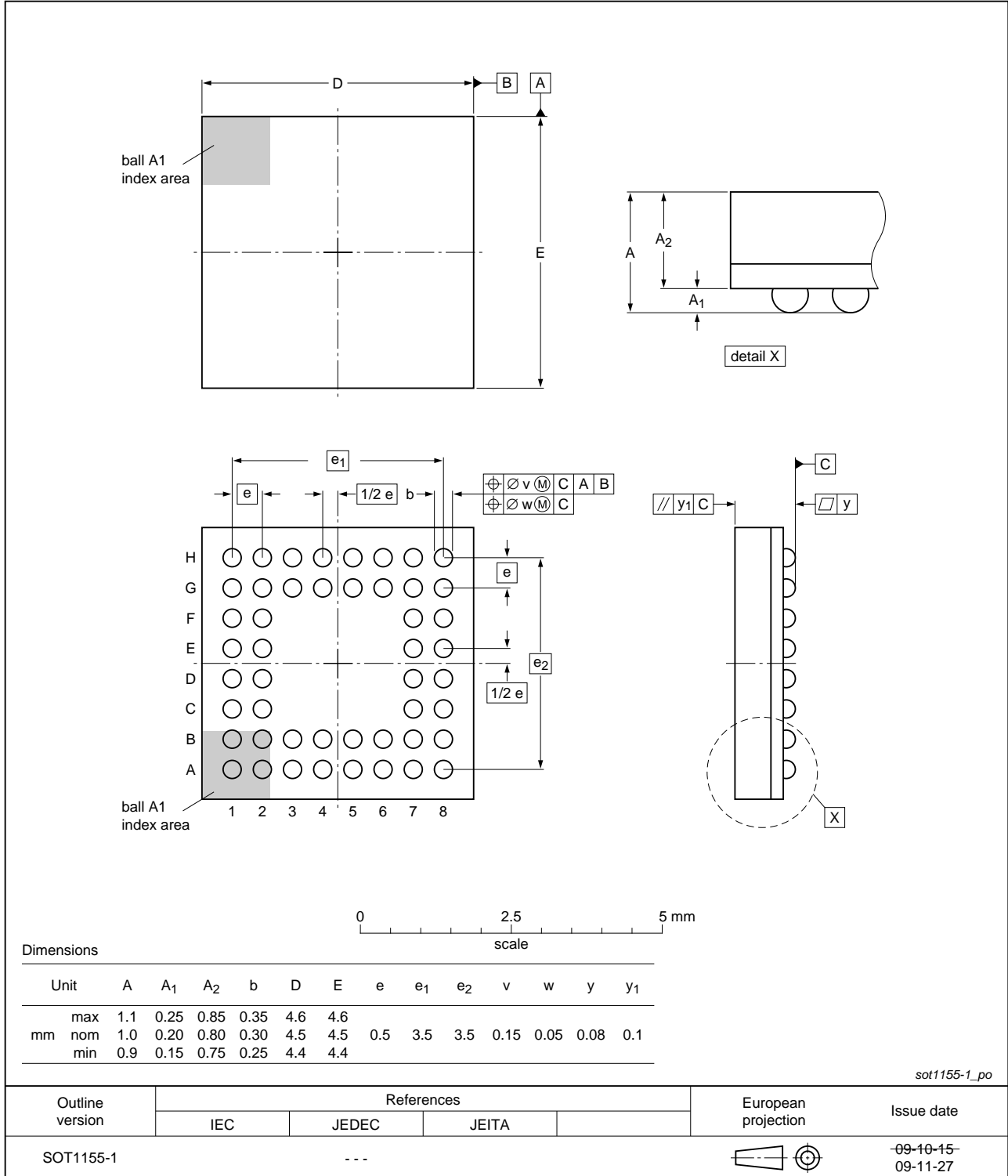


Fig 4. Package outline TFBGA48 (SOT1155-1)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 5](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 8](#) and [9](#)

Table 8. SnPb eutectic process (from J-STD-020C)

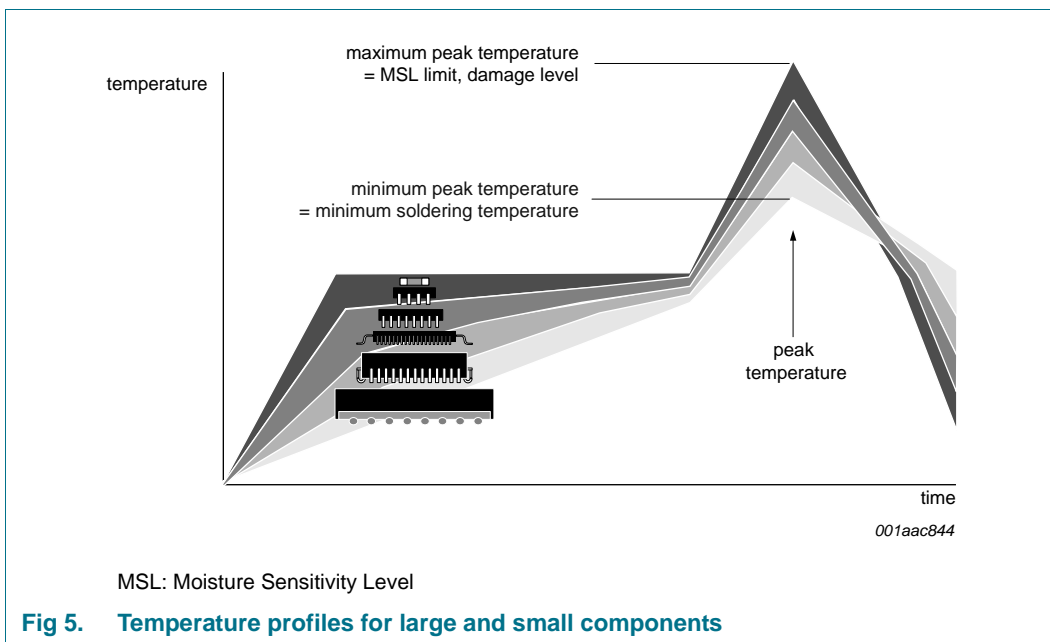
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 9. Lead-free process (from J-STD-020C)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 5](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

14. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged-Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DDR2 | Double Data Rate 2 |
| DDR3 | Double Data Rate 3 |
| DRAM | Dynamic Random Access Memory |
| ESD | ElectroStatic Discharge |
| FET | Field-Effect Transistor |
| HBM | Human Body Model |
| I/O | Input/Output |
| MT/s | Mega Transfers per second |
| SSTL_15 | Stub Series Terminated Logic for 1.5 V |
| SSTL_18 | Stub Series Terminated Logic for 1.8 V |

15. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|--------------------|---------------|----------------|
| CBTW28DD14 v.2 | 20120726 | Product data sheet | - | CBTW28DD14 v.1 |
| Modifications: | • Section 7.1 "Function selection" : added second paragraph | | | |
| CBTW28DD14 v.1 | 20100720 | Product data sheet | - | - |

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| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
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