3.5A, 1.2MHz, Synchronous Step-Down Converter

General Description

The RT8086B is a high efficiency, synchronous step-down DC/DC converter. The available input voltage range is from 2.8V to 5.5V and the regulated output voltage is adjustable from 0.6V to 3.3V while delivering up to 3.5A of output current.

The internal synchronous low on-resistance power switches increase efficiency and eliminate the need for an external Schottky diode.

The current mode constant on-time operation with internal compensation allows the transient response to be optimized over a wide range of loads and output capacitors. TheRT8086B is available in the UQFN-12L 2x2 (FC) package.

Ordering Information

RT8086B □□

- Package Type
  QUF : UQFN-12L 2x2 (FC) (U-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

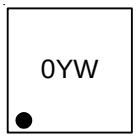
Features

- **High Efficiency Up to 95%**
- **Low $R_{DS(ON)}$ Switches : 50mΩ/40mΩ**
- **0.6V Reference Allows for Low Output Voltage**
- **Internal Compensation**
- **Input Voltage Range : 2.8V to 5.5V**
- **Adjustable Output Voltage from 0.6V to 3.3V**
- **1.2MHz Switching Frequency**
- **Start-Up into Pre-Biased Load**
- **Built in Soft-Start**
- **Power Good Indication**
- **Cycle-by-Cycle Current Limit**
- **Input Under Voltage Lockout**
- **Output Under Voltage Protection (Hiccup)**
- **Thermal Shutdown Protection**
- **RoHS Compliant and Halogen Free**

Applications

- Smart Handheld devices
- Portable Instruments
- Battery-Powered Equipment
- Distributed Power Systems

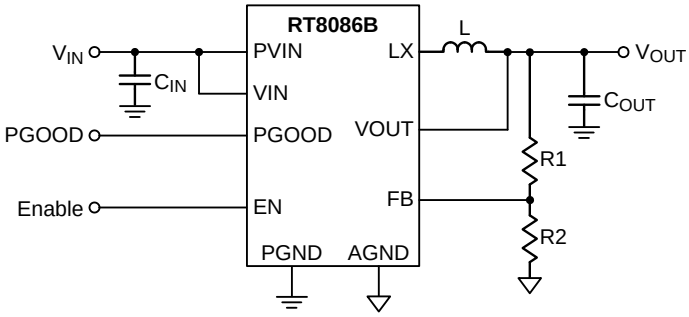
Marking Information



0Y : Product Code

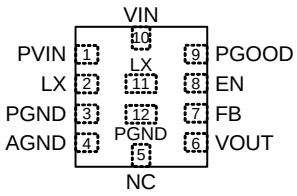
W : Date Code

Simplified Application Circuit



Pin Configurations

(TOP VIEW)

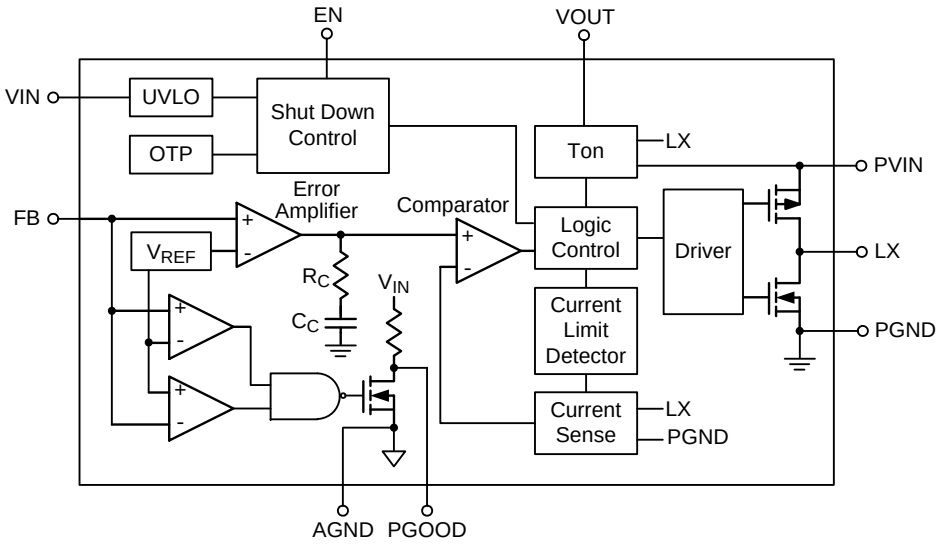


UQFN-12L 2x2 (FC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PVIN	Power Input. The available input voltage range is from 2.8V to 5.5V. A 10μF or larger input capacitor is needed to reduce voltage spikes at the input.
2, 11	LX	Switch Node. Output of the internal high side and low side MOSFETs.
3, 12	PGND	Power Ground.
4	AGND	Analog Ground.
5	NC	No Internal Connection.
6	VOUT	Sense Input Pin for Output Voltage.
7	FB	Feedback Input. This pin used to set the output voltage of the converter to regulate to the desired value via an external resistive divider. The feedback reference voltage is 0.6V typically.
8	EN	Enable Control Input. A logic-high (1.2V < EN < 5.5V) enables the converter; a logic-low forces the IC into shutdown mode.
9	PGOOD	Power Good Indicator. The output of this pin is an open drain with internal pull-up resister to VIN. The output of this pin is pulled to high when the FB voltage is within 10%; otherwise it is Low.
10	VIN	Supply Voltage for Internal Control Circuit. It is connected to PVIN inside the chip.

Function Block Diagram



Operation

The RT8086B is a synchronous low voltage step-down converter that can support the input voltage range from 2.8V to 5.5V and the output current can be up to 3.5A. The RT8086B uses a constant on-time, current mode architecture. In normal operation, the high side P-MOSFET is turned on when the switch controller is set by the comparator and is turned off when the Ton comparator resets the switch controller.

Low side MOSFET peak current is measured by internal RSENSE. The error amplifier EA adjusts COMP voltage by comparing the feedback signal (V_{FB}) from the output voltage with the internal 0.6V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, then the COMP voltage rises to allow higher inductor current to match the load current.

UV Comparator

If the feedback voltage (V_{FB}) is lower than threshold voltage 0.2V, the UV comparator's output will go high and the switch controller will turn off the high side MOSFET. The output under voltage protection is designed to operate in Hiccup mode.

PGOOD Comparator

When the feedback voltage (V_{FB}) is higher than threshold voltage 0.54V and under 0.66V, the PGOOD open drain output will be high impedance.

Enable Comparator

A logic-high enables the converter; a logic-low forces the IC into shutdown mode. There is an internal pull down 1MΩ resistor at EN pin.

Soft-Start (SS)

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The V_{FB} voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is 2ms.

Over Current Protection (OCP)

The RT8086B provides over current protection by detecting low side MOSFET valley inductor current. If the sensed valley inductor current is over the current limit threshold (4.5A typ.), the OCP will be triggered. When OCP is tripped, the RT8086B will keep the over current threshold level until the over current condition is removed.

Thermal Shutdown (OTP)

The device implements an internal thermal shutdown function when the junction temperature exceeds 140°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal shutdown threshold. Once the die temperature decreases below the hysteresis of 20°C, the device reinstates the power up sequence.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, PVIN, VIN ---------- –0.3V to 6.5V
- Switch Node Voltage, LX ---------- –0.3V to (PVIN + 0.3V)
- Other Pins Voltage ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  UQFN-12L 2x2 (FC) ---------- 1.25W
- Package Thermal Resistance (Note 2)
  UQFN-12L 2x2 (FC), θ_{JA} ---------- 80°C/W
  UQFN-12L 2x2 (FC), θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.8V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		PVIN		2.8	--	5.5	V
Feedback Reference Voltage		V_{REF}		0.588	0.6	0.612	V
Feedback Leakage Current		I_{FB}	V_{FB} = 3.3V	--	--	1	μA
Quiescent Current			Close loop, no load current	--	60	--	μA
Shutdown Current			Shutdown	--	--	1	
Output Voltage Line Regulation			V_{IN} = 2.8V to 5.5V	--	0.1	--	%/V
Output Voltage Load Regulation			V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 0A to 3.5A	--	0.4	--	%
Switching Frequency			V_{IN} = 5V, V_{OUT} = 1.2V	--	1.2	--	MHz
Switch On-Resistance	High-Side	R_{PMOS}	I_{LX} = 0.3A, V_{IN} = 5V	--	50	--	mΩ
	Low-Side	R_{NMOS}	I_{LX} = 0.3A, V_{IN} = 5V	--	40	--	
Current Limit		I_{LIM}	Valley current	4.5	--	--	A
Min. Off-Time		t_{OFF}		--	100	--	ns
Under Voltage Lockout Threshold			V_{IN} Rising	--	2.5	--	V
			V_{IN} Falling	--	2.2	--	
Thermal Shutdown				--	140	--	°C
Enable Voltage	Logic-High			1.2	--	5.5	V
	Logic-Low			--	--	0.4	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN Input Current		V_{EN} = 2V	--	2	--	μA
		V_{EN} = 0V	--	0	--	
PGOOD Pin Trigger Delay			--	90	--	μs
PGOOD Pin Threshold (Relative to VOUT)		FB with respect to the Regulation	--	±10	--	%
PGOOD Open Drain Impedance	R_{PGOOD}	PGOOD = PVIN	--	500	--	kΩ
PGOOD On-Resistance Impedance		PGOOD = Low	--	--	100	Ω
Soft-Start Time	T_{SS}		--	2	--	ms
On-Time	T_{ON}	V_{IN} = 5V, V_{OUT} = 1.2V	--	200	--	ns
		V_{IN} = 3.6V, V_{OUT} = 1.2V	--	277	--	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

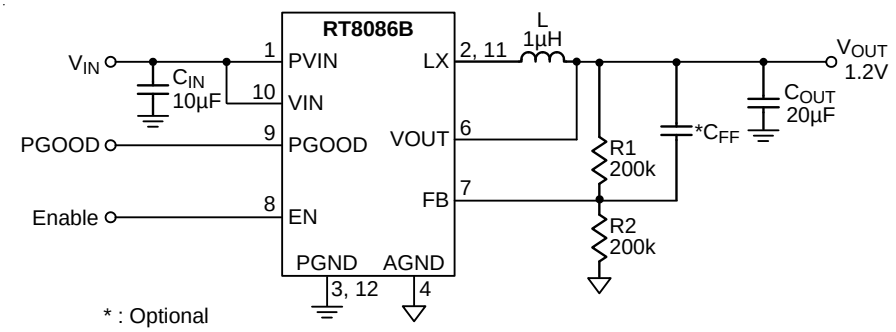
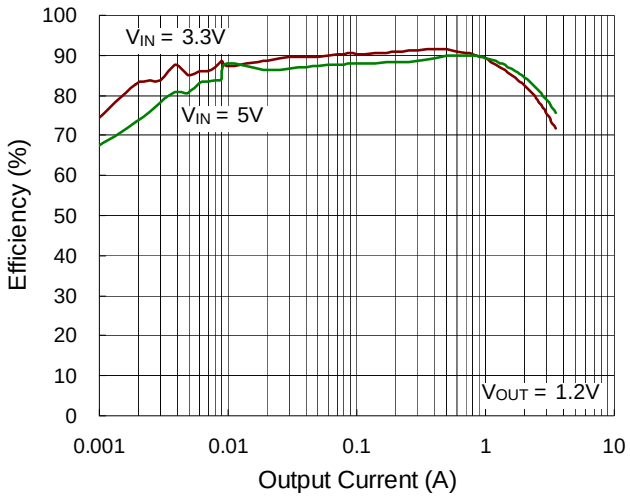


Table 1. Suggested Component Values

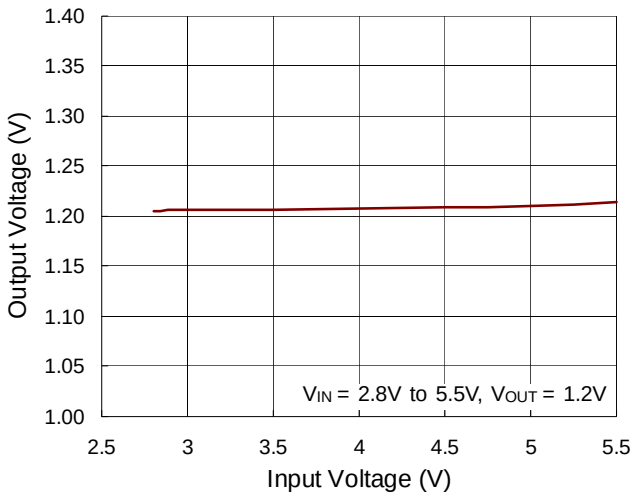
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (µH)	C_{OUT} (µF)
1.2V	200	200	1	20
1.8V	200	100	1	20
2.5V	200	63.4	1	20
3.3V	200	44.2	1	20

Typical Operating Characteristics

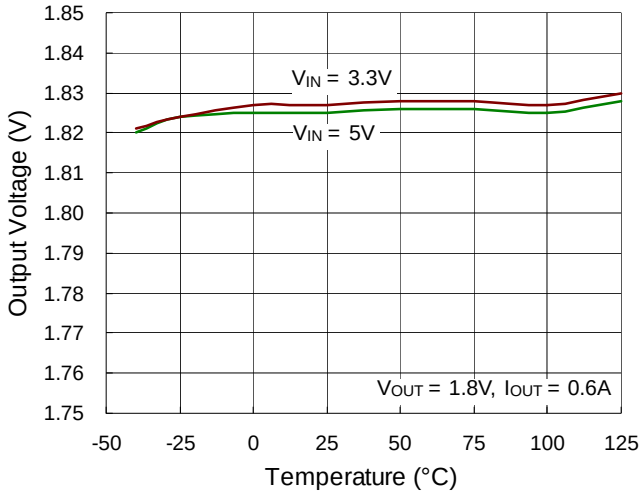
Efficiency vs. Output Current



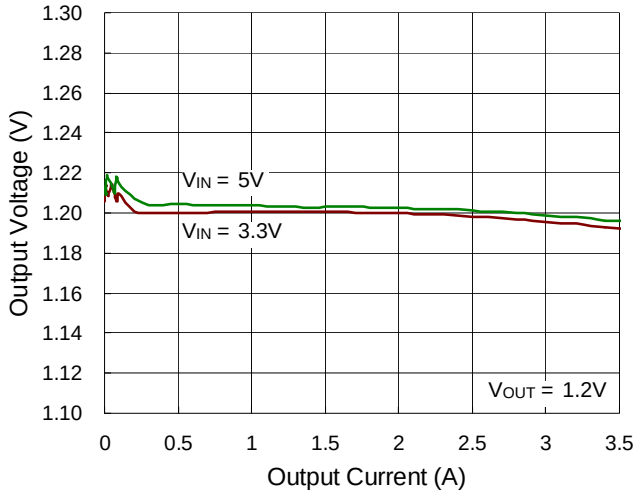
Output Voltage vs. Input Voltage



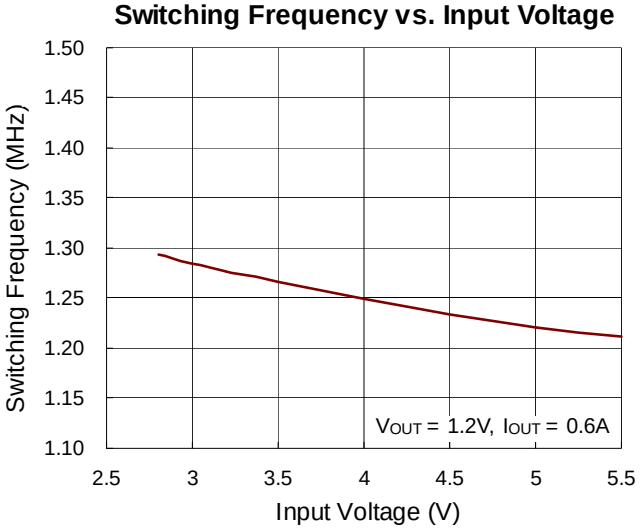
Output Voltage vs. Temperature



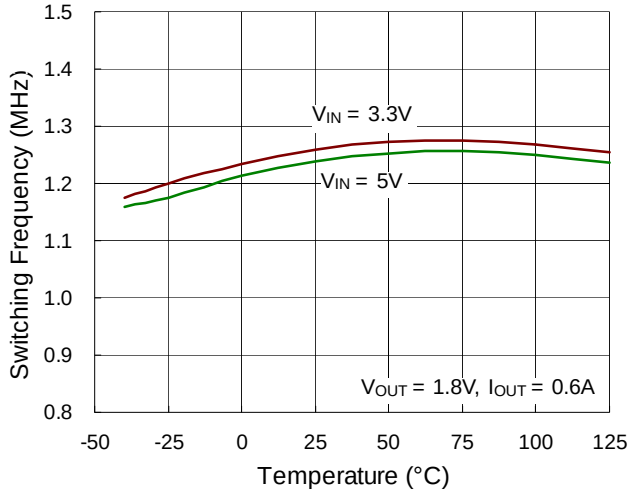
Output Voltage vs. Output Current



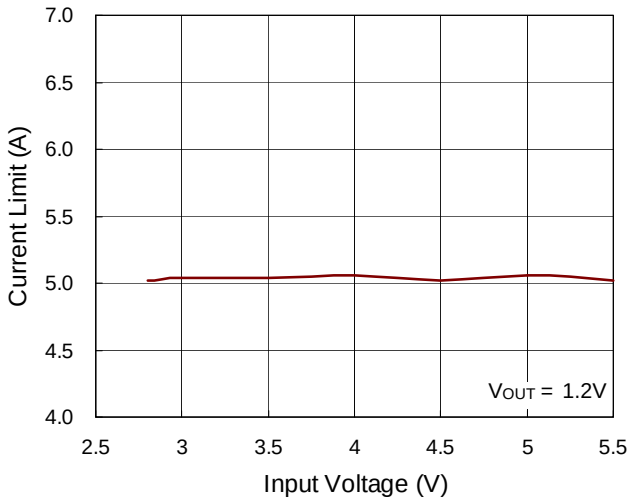
Switching Frequency vs. Input Voltage



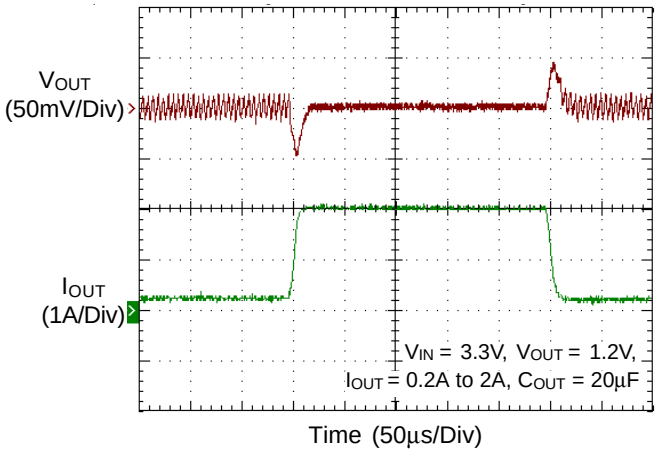
Switching Frequency vs. Temperature



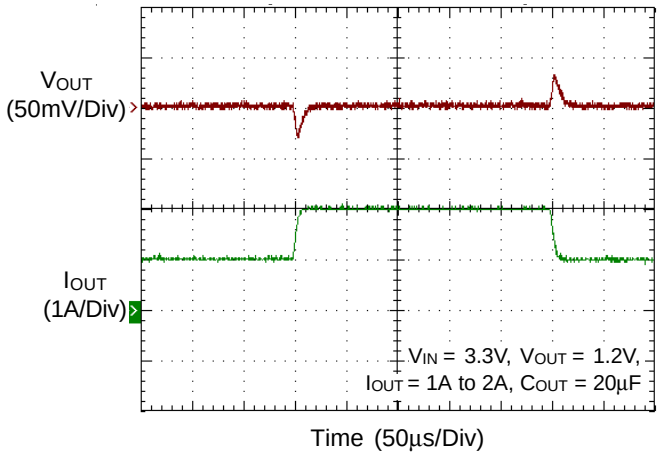
Current Limit vs. Input Voltage



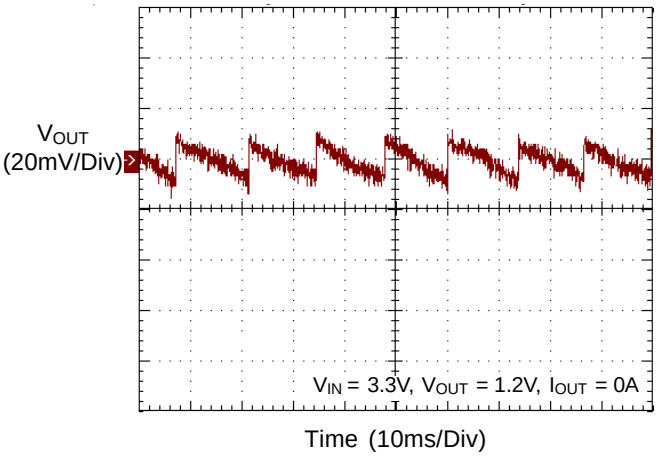
Load Transient Response



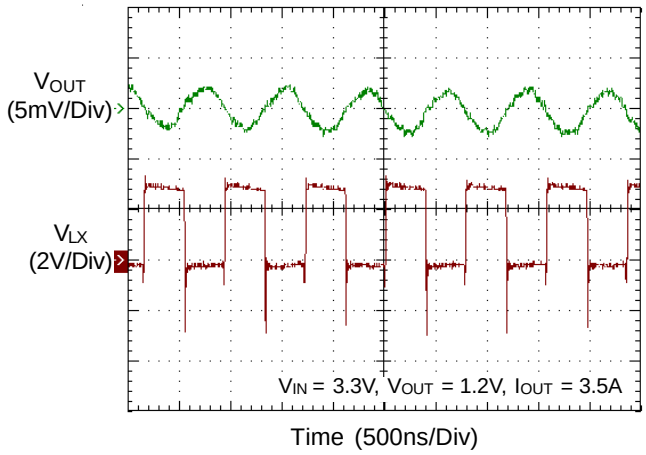
Load Transient Response



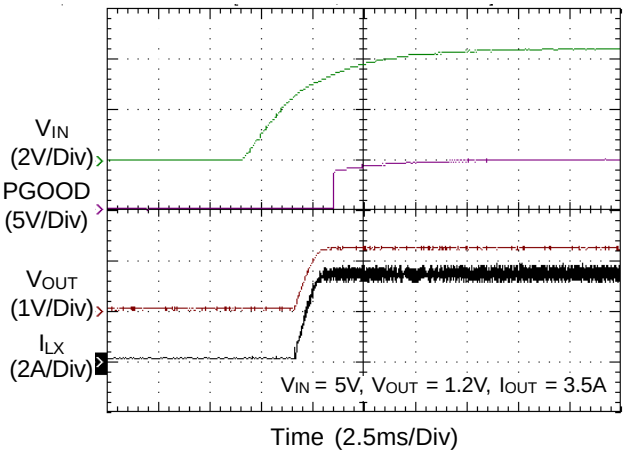
Output Ripple Voltage



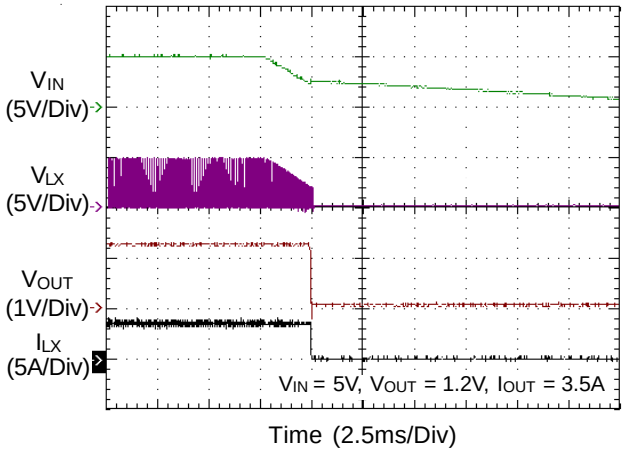
Output Ripple Voltage



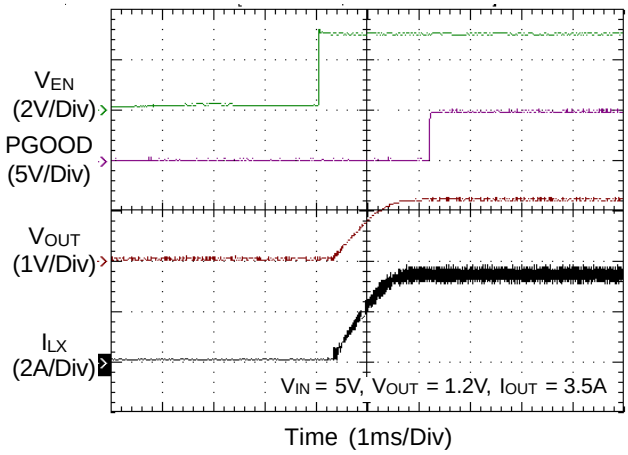
Power On from VIN



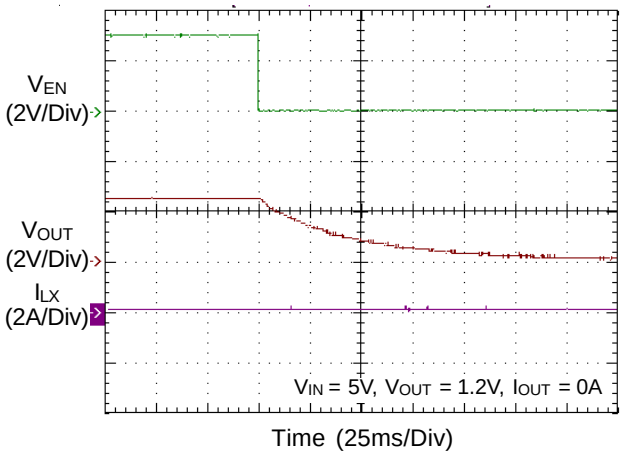
Power Off from VIN



Power On from EN



Power Off from EN



Application Information

The RT8086B is a single-phase step-down converter. It provides single feedback loop, current mode control with fast transient response. An internal 0.6V reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed switching frequency (1.2MHz) oscillator and internal compensation are integrated to minimize external component count. Protection features include over current protection, under voltage protection and over temperature protection.

Output Voltage Setting

Connect a resistive voltage divider at the FB between V_{OUT} and GND to adjust the output voltage. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is the feedback reference voltage 0.6V (typ.).

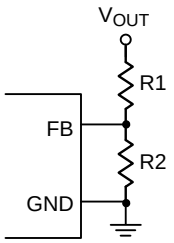


Figure 1. Setting V_{OUT} with a Voltage Divider

Chip Enable and Disable

The EN pin allows for power sequencing between the controller bias voltage and another voltage rail. The RT8086B remains in shutdown if the EN pin is lower than 400mV. When the EN pin rises above the V_{EN} trip point, the RT8086B begins a new initialization and soft-start cycle.

Internal Soft-Start

The RT8086B provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, the internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the voltage at the FB pin, causing PWM pulse width to increase slowly and in turn reduce the input surge current. The internal 0.6V reference takes over the loop control once the internal ramping-up voltage becomes higher than 0.6V.

UVLO Protection

The RT8086B has input Under Voltage Lockout protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (2.5V typ.), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will stop switching. The UVLO rising and falling threshold voltage has a hysteresis to prevent noise-caused reset.

Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times LIR \times I_{LOAD(MAX)} \times V_{IN}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current.

Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2} \times I_{LOAD(MAX)}\right)$$

The calculation above serves as a general reference. To further improve transient response, the output inductor can be further reduced. This relation should be considered along with the selection of the output capacitor.

Input Capacitor Selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 10µF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability.

Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{IN\_RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is selecting a proper capacitor for RMS current rating. One good design uses more than one capacitor with low equivalent series resistance (ESR) in parallel to form a capacitor bank.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor and the inductor form a low pass filter in the Buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in ripple voltage. The output voltage ripple (V_{P-P}) can be calculated by the following equation :

$$V_{P\_P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}}\right)$$

When load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage undershoot (V_{SAG}) can be calculated by the following equation :

$$V_{SAG} = \Delta I_{LOAD} \times ESR$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, the ESL contributes to part of the voltage sag. Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For UQFN-12L 2x2(FC) package, the thermal resistance, θ_{JA}, is 80°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (80°C/W) = 1.25W for UQFN-12L 2x2 (FC) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

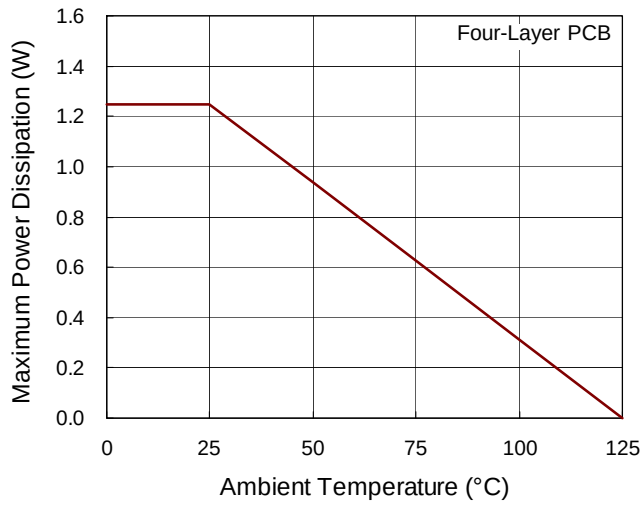


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout. Certain points must be considered before starting a layout using the RT8086B.

- Make the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (V_{IN} and GND).
- LX node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the LX node to prevent stray capacitive noise pick-up.
- Ensure all feedback network connections are short and direct. Place the feedback network as close to the chip as possible.
- The GND pin and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.
- An example of PCB layout guide is shown in Figure 3 for reference.

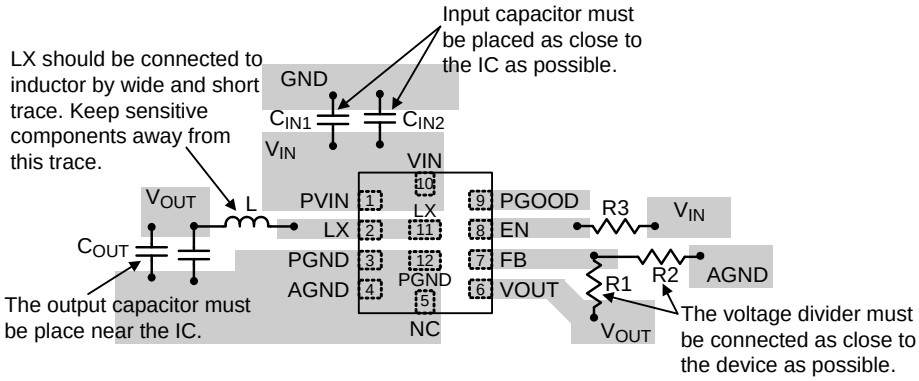
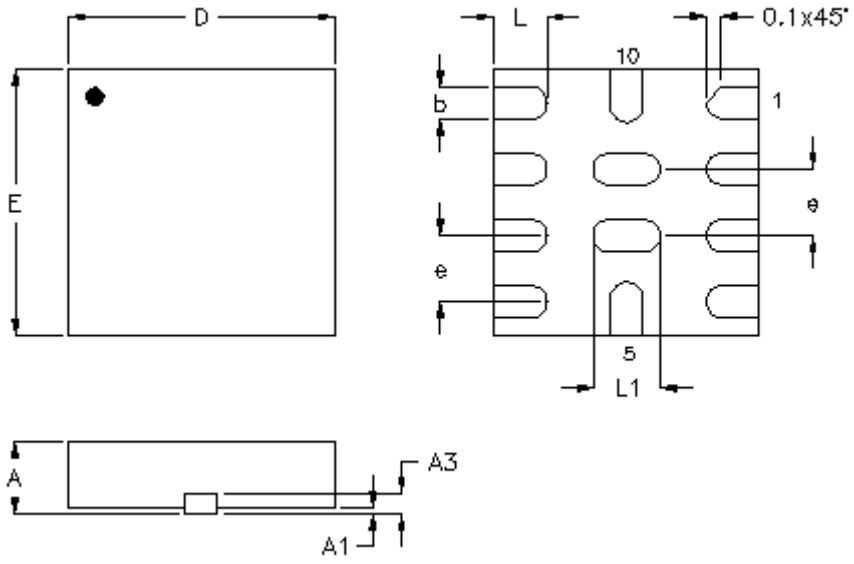


Figure 3. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.152	0.004	0.006
b	0.200	0.300	0.008	0.012
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
e	0.500		0.020	
L	0.350	0.450	0.014	0.018
L1	0.450	0.550	0.018	0.022

U-Type 12L QFN 2x2 (FC) Package

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