

# FDP7N50F / FDPF7N50F

## N-Channel MOSFET, FRFET

### 500V, 6A, 1.15Ω

#### Features

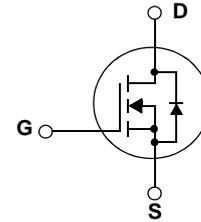
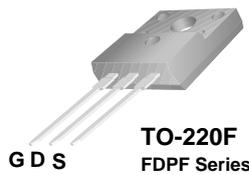
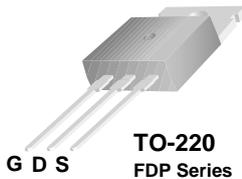
- $R_{DS(on)} = 0.95\Omega$  (Typ.) @  $V_{GS} = 10V, I_D = 3A$
- Low gate charge (Typ. 15nC)
- Low  $C_{rss}$  (Typ. 6.3pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant



#### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advance technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switching mode power supplies and active power factor correction.



#### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted\*

Symbol	Parameter	FDP7N50F	FDPF7N50F	Units
$V_{DSS}$	Drain to Source Voltage	500		V
$V_{GSS}$	Gate to Source Voltage	±30		V
$I_D$	Drain Current	-Continuous ( $T_C = 25^\circ\text{C}$ )	6	6*
		-Continuous ( $T_C = 100^\circ\text{C}$ )	3.6	3.6*
$I_{DM}$	Drain Current	- Pulsed (Note 1)	24	24*
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	270	mJ
$I_{AR}$	Avalanche Current	(Note 1)	6	A
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	20	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	200	38.5
		- Derate above $25^\circ\text{C}$	1.59	0.3
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$

\*Drain current limited by maximum junction temperature

#### Thermal Characteristics

Symbol	Parameter	FDP7N50F	FDPF7N50F	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	4.0	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Junction to Ambient	0.5	-	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	62.5	

**Package Marking and Ordering Information**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP7N50F	FDP7N50F	TO-220	-	-	50
FDPF7N50F	FDPF7N50F	TO-220F	-	-	50

**Electrical Characteristics**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
--------	-----------	-----------------	------	------	------	-------

**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.5	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 400\text{V}, T_C = 125^\circ\text{C}$	-	-	10 100	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 3\text{A}$	-	0.95	1.15	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{V}, I_D = 3\text{A}$ (Note 4)	-	4.3	-	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	720	960	pF
$C_{oss}$	Output Capacitance		-	85	115	pF
$C_{rss}$	Reverse Transfer Capacitance		-	6.3	10	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400\text{V}, I_D = 6\text{A}$ $V_{GS} = 10\text{V}$ (Note 4, 5)	-	15	20	nC
$Q_{gs}$	Gate to Source Gate Charge		-	4.5	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	6	-	nC

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{V}, I_D = 6\text{A}$ $R_G = 25\Omega$ (Note 4, 5)	-	17	45	ns
$t_r$	Turn-On Rise Time		-	30	70	ns
$t_{d(off)}$	Turn-Off Delay Time		-	35	80	ns
$t_f$	Turn-Off Fall Time		-	20	50	ns

**Drain-Source Diode Characteristics**

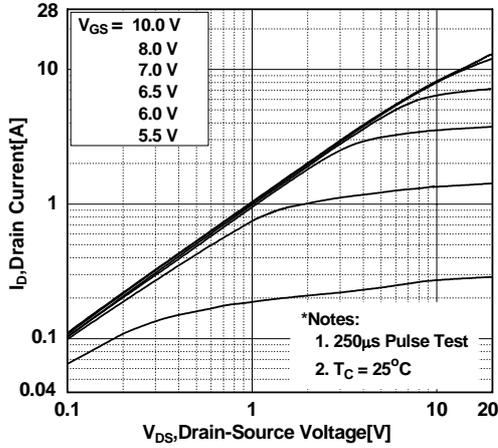
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	6	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	24	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 6\text{A}$	-	-	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 6\text{A}$	-	85	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$ (Note 4)	-	0.15	-	$\mu\text{C}$

**Notes:**

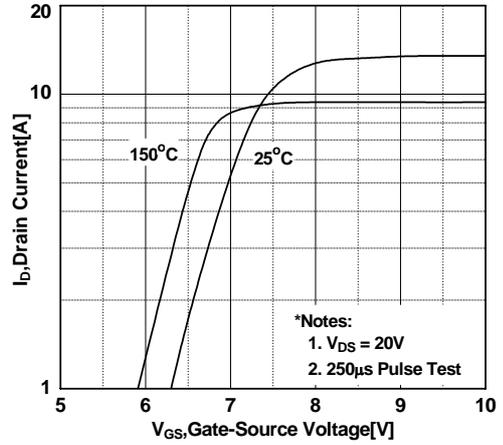
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $L = 13\text{mH}, I_{AS} = 6\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 6\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

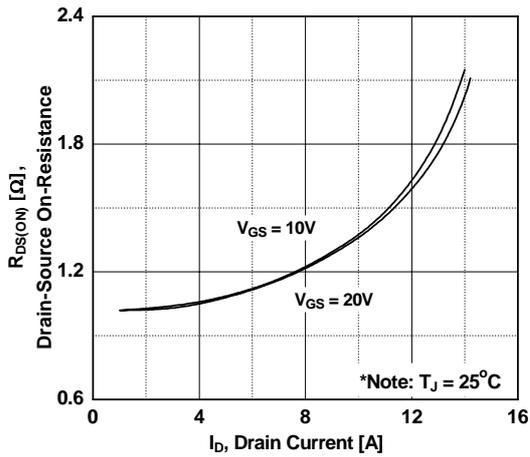
**Figure 1. On-Region Characteristics**



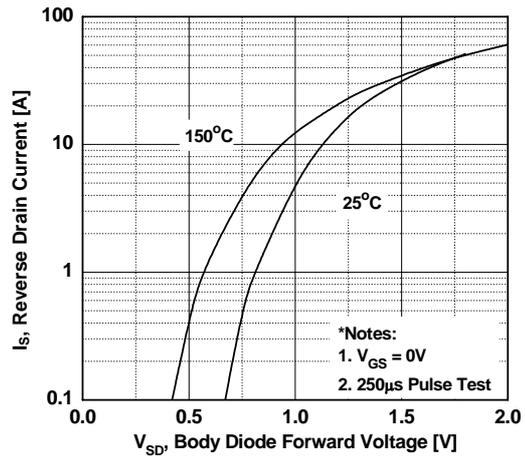
**Figure 2. Transfer Characteristics**



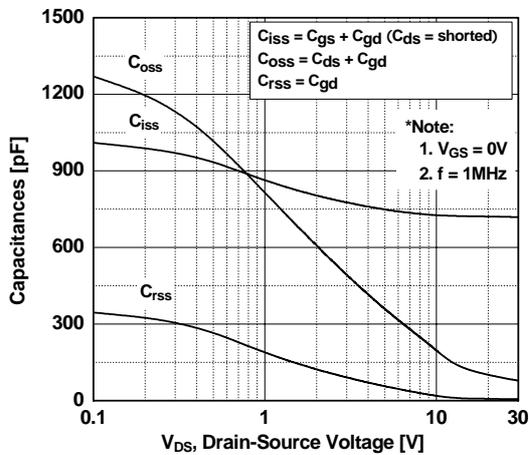
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



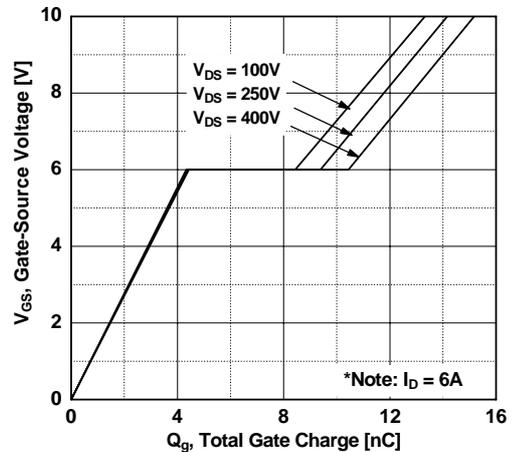
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

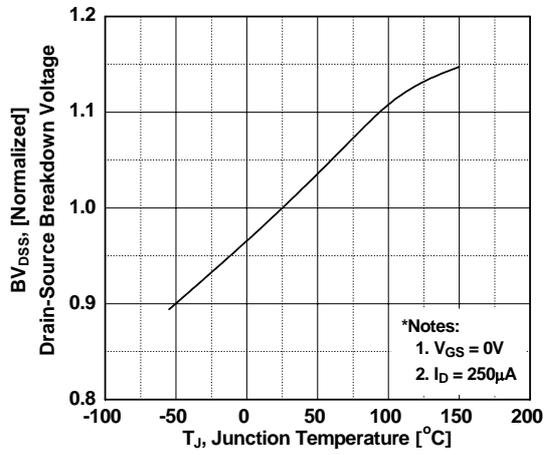


**Figure 6. Gate Charge Characteristics**

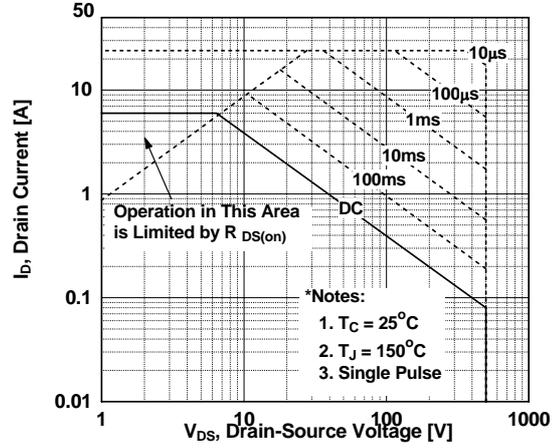


**Typical Performance Characteristics** (Continued)

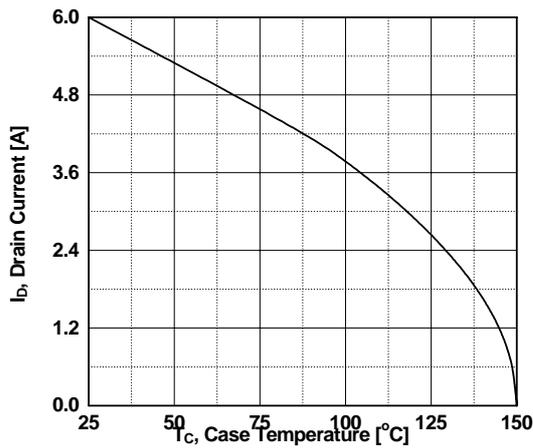
**Figure 7. Breakdown Voltage Variation vs. Temperature**



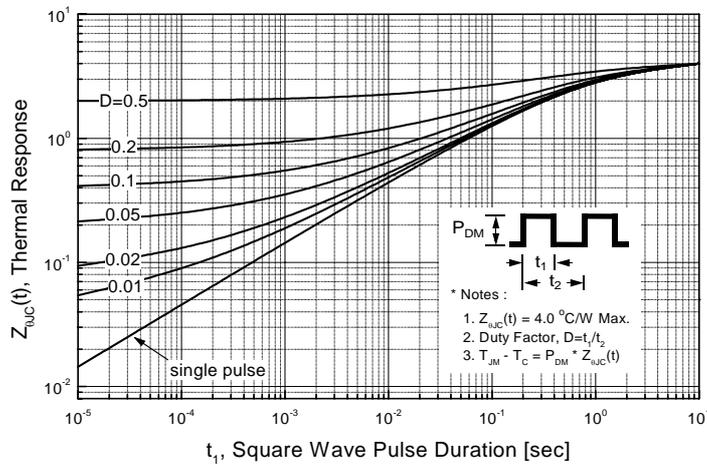
**Figure 8. Maximum Safe Operating Area - FDPF7N50F**



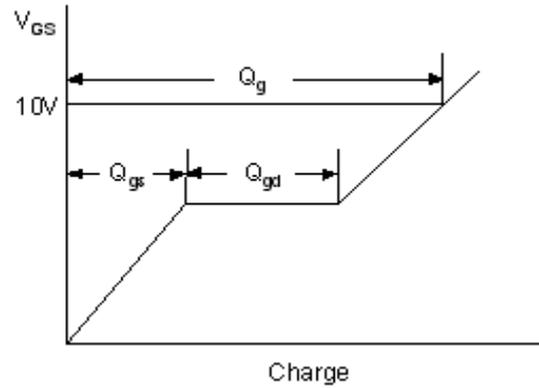
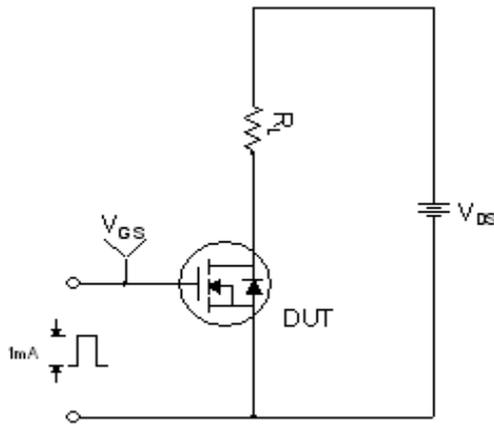
**Figure 9. Maximum Drain Current vs. Case Temperature - FDPF7N50F**



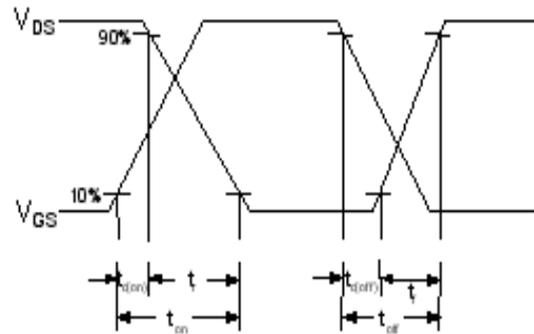
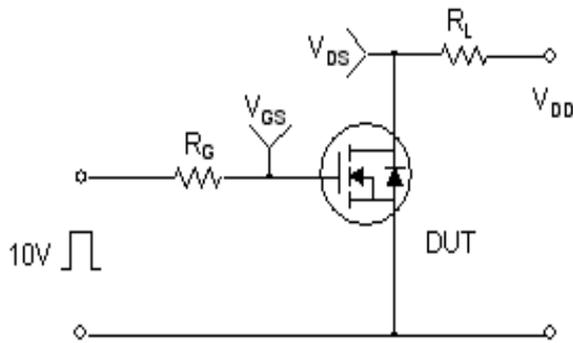
**Figure 10. Transient Thermal Response Curve - FDPF7N50F**



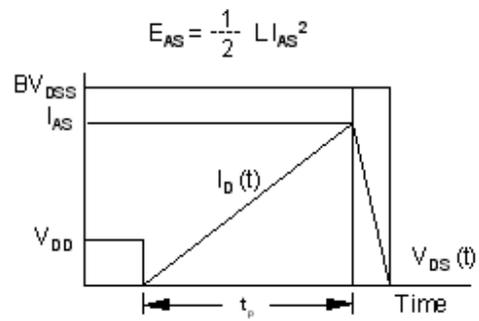
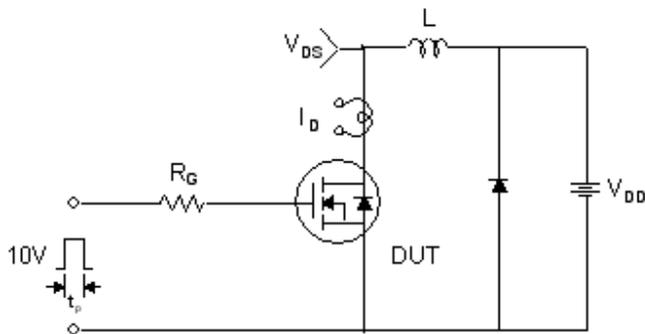
**Gate Charge Test Circuit & Waveform**



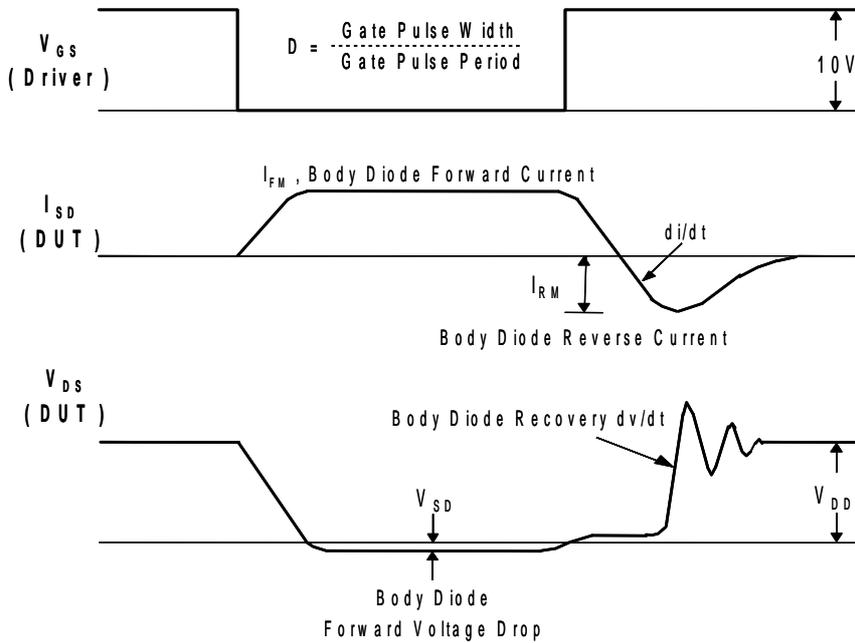
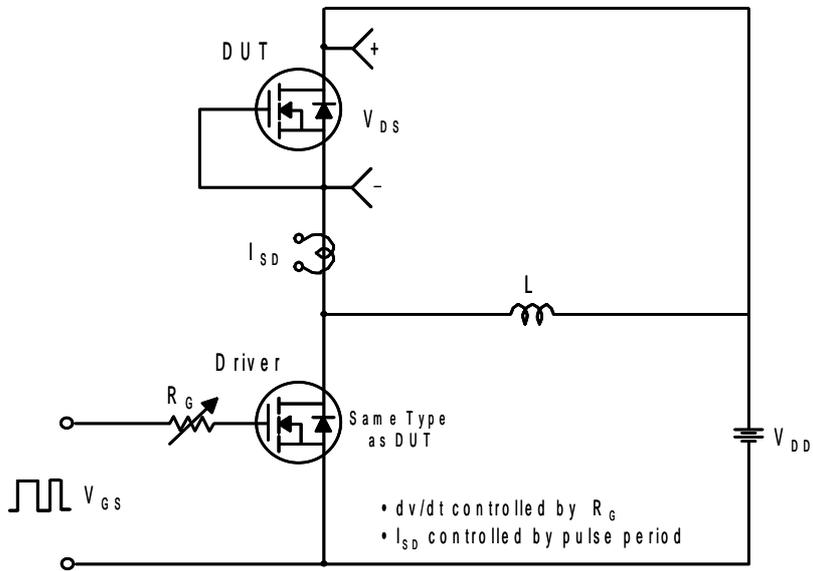
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**



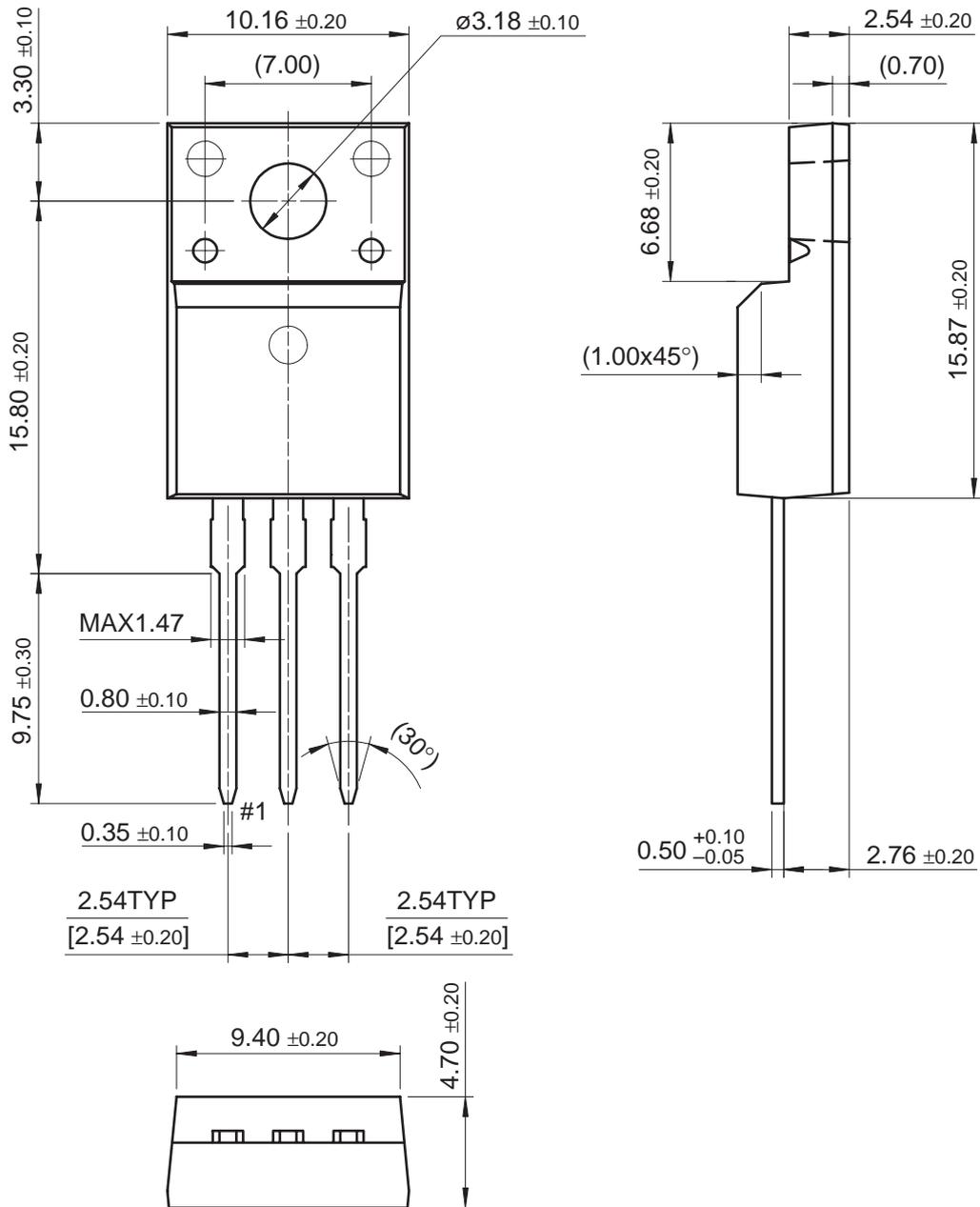
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Mechanical Dimensions

TO-220F



Dimensions in Millimeters



### TRADEMARKS

The following are registered and unregistered trademarks and service marks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx <sup>®</sup>	Green FPS <sup>™</sup>	Power247 <sup>®</sup>	SuperSOT <sup>™</sup> -8
Build it Now <sup>™</sup>	Green FPS <sup>™</sup> e-Series <sup>™</sup>	POWEREDGE <sup>®</sup>	SyncFET <sup>™</sup>
CorePLUS <sup>™</sup>	GTO <sup>™</sup>	Power-SPM <sup>™</sup>	The Power Franchise <sup>®</sup>
CROSSVOLT <sup>™</sup>	<i>i-Lo</i> <sup>™</sup>	PowerTrench <sup>®</sup>	<b>the power</b> franchise
CTL <sup>™</sup>	IntelliMAX <sup>™</sup>	Programmable Active Droop <sup>™</sup>	TinyBoost <sup>™</sup>
Current Transfer Logic <sup>™</sup>	ISOPLANAR <sup>™</sup>	QFET <sup>®</sup>	TinyBuck <sup>™</sup>
EcoSPARK <sup>®</sup>	MegaBuck <sup>™</sup>	QST <sup>™</sup>	TinyLogic <sup>®</sup>
<b>F</b> <sup>®</sup>	MICROCOUPLER <sup>™</sup>	QT Optoelectronics <sup>™</sup>	TINYOPTO <sup>™</sup>
Fairchild <sup>®</sup>	MicroFET <sup>™</sup>	Quiet Series <sup>™</sup>	TinyPower <sup>™</sup>
Fairchild Semiconductor <sup>®</sup>	MicroPak <sup>™</sup>	RapidConfigure <sup>™</sup>	TinyPWM <sup>™</sup>
FACT Quiet Series <sup>™</sup>	MillerDrive <sup>™</sup>	SMART START <sup>™</sup>	TinyWire <sup>™</sup>
FACT <sup>®</sup>	Motion-SPM <sup>™</sup>	SPM <sup>®</sup>	μSerDes <sup>™</sup>
FAST <sup>®</sup>	OPTOLOGIC <sup>®</sup>	STEALTH <sup>™</sup>	UHC <sup>®</sup>
FastvCore <sup>™</sup>	OPTOPLANAR <sup>®</sup>	SuperFET <sup>™</sup>	UniFET <sup>™</sup>
FPS <sup>™</sup>	 <sup>®</sup>	SuperSOT <sup>™</sup> -3	VCX <sup>™</sup>
FRFET <sup>®</sup>	PDP-SPM <sup>™</sup>	SuperSOT <sup>™</sup> -6	
Global Power Resource <sup>SM</sup>	Power220 <sup>®</sup>		

### DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### PRODUCT STATUS DEFINITIONS

#### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I31