International
IOR Rectifier

PD - 94648

IRFR3707Z
IRFU3707Z

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max	Qg
30V	9.5mΩ	9.6nC

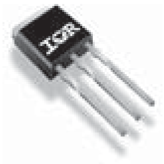
Applications

- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use

Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current


D-Pak
IRFR3707Z


I-Pak
IRFU3707Z

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	56④	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	39④	
I_{DM}	Pulsed Drain Current ①	220	
P_D @T_C = 25°C	Maximum Power Dissipation	50	W
P_D @T_C = 100°C	Maximum Power Dissipation	25	
	Linear Derating Factor	0.33	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑤	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Notes ① through ⑤ are on page 11

04/03/03

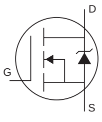
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.023	–––	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	7.5	9.5	mΩ	V_{GS} = 10V, I_D = 15A ③
		–––	10	12.5		V_{GS} = 4.5V, I_D = 12A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.80	2.25	V	$V_{DS} = V_{GS}$, I_D = 250µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	–––	-5.0	–––	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	1.0	µA	V_{DS} = 24V, V_{GS} = 0V
		–––	–––	150		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -20V
gfs	Forward Transconductance	71	–––	–––	S	V_{DS} = 15V, I_D = 12A
Q_g	Total Gate Charge	–––	9.6	14	nC	V_{DS} = 15V V_{GS} = 4.5V I_D = 12A See Fig. 16
Q_{gs1}	Pre-Vth Gate-to-Source Charge	–––	2.6	–––		
Q_{gs2}	Post-Vth Gate-to-Source Charge	–––	0.90	–––		
Q_{gd}	Gate-to-Drain Charge	–––	3.5	–––		
Q_{godr}	Gate Charge Overdrive	–––	2.6	–––		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	–––	4.4	–––		
Q_{oss}	Output Charge	–––	5.8	–––	nC	V_{DS} = 15V, V_{GS} = 0V
$t_{d(on)}$	Turn-On Delay Time	–––	8.0	–––	ns	V_{DD} = 16V, V_{GS} = 4.5V ③ I_D = 12A Clamped Inductive Load
t_r	Rise Time	–––	11	–––		
$t_{d(off)}$	Turn-Off Delay Time	–––	12	–––		
t_f	Fall Time	–––	3.3	–––		
C_{iss}	Input Capacitance	–––	1150	–––	pF	V_{GS} = 0V V_{DS} = 15V f = 1.0MHz
C_{oss}	Output Capacitance	–––	260	–––		
C_{rss}	Reverse Transfer Capacitance	–––	120	–––		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	–––	42	mJ
I_{AR}	Avalanche Current ①	–––	12	A
E_{AR}	Repetitive Avalanche Energy ①	–––	5.0	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	56④	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	220		
V_{SD}	Diode Forward Voltage	–––	–––	1.0	V	T_J = 25°C, I_S = 12A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	–––	25	38	ns	T_J = 25°C, I_F = 12A, V_{DD} = 15V di/dt = 100A/µs ③
Q_{rr}	Reverse Recovery Charge	–––	17	26	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

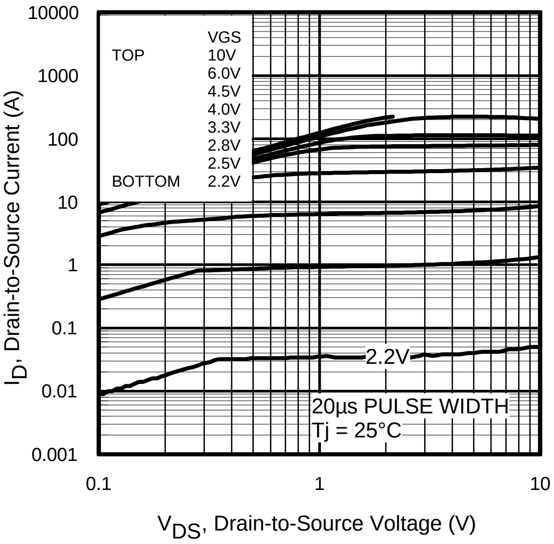


Fig 1. Typical Output Characteristics

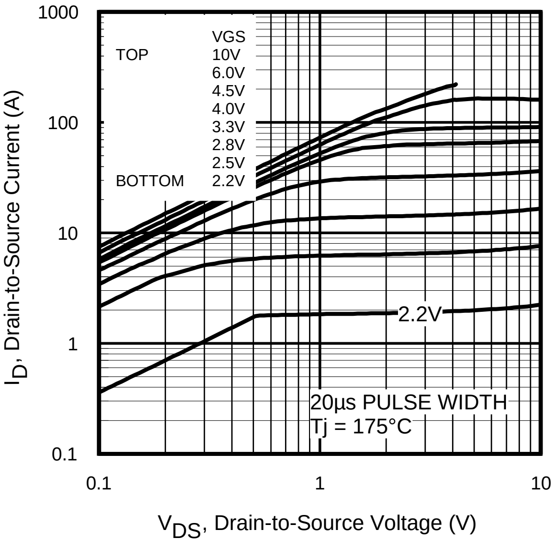


Fig 2. Typical Output Characteristics

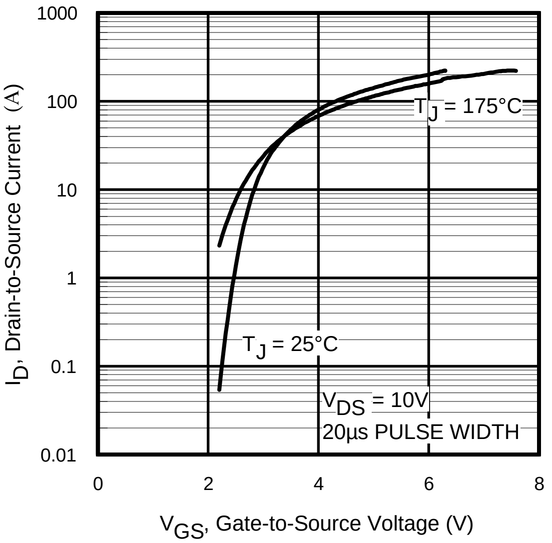


Fig 3. Typical Transfer Characteristics

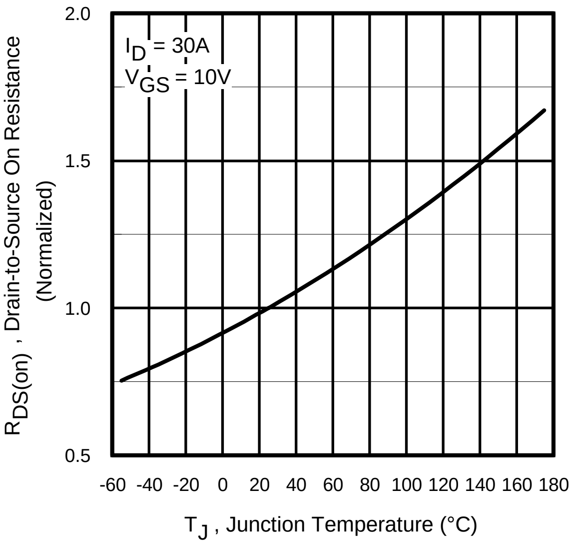


Fig 4. Normalized On-Resistance
vs. Temperature

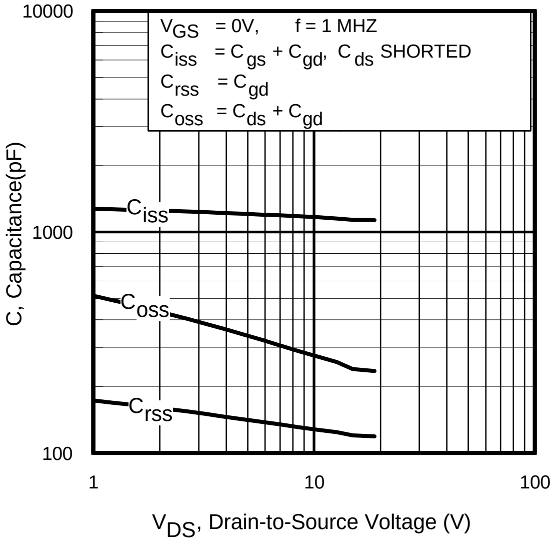


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

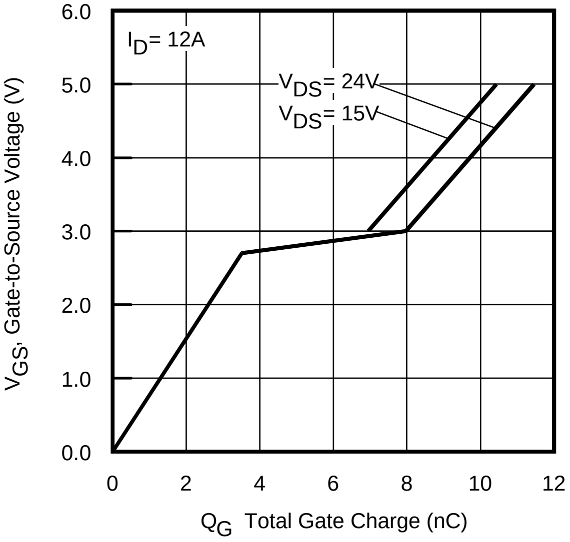


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

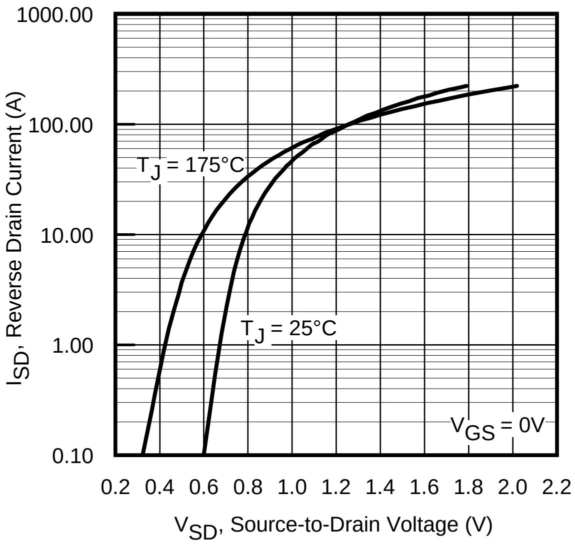


Fig 7. Typical Source-Drain Diode Forward Voltage

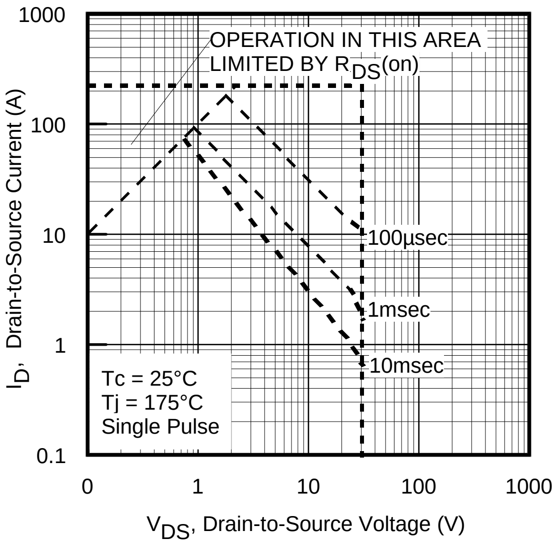


Fig 8. Maximum Safe Operating Area

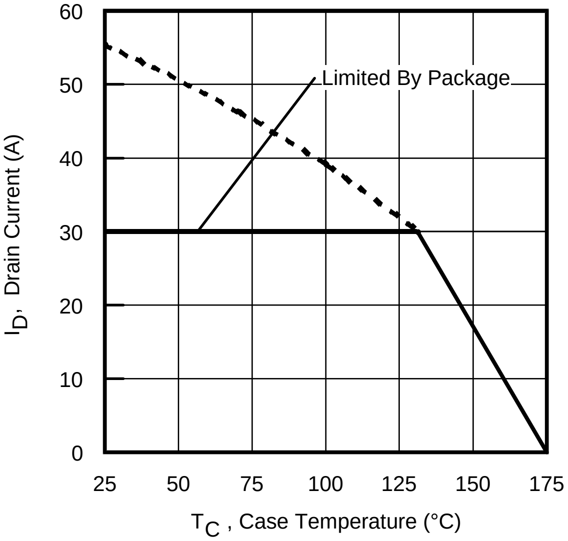


Fig 9. Maximum Drain Current vs. Case Temperature

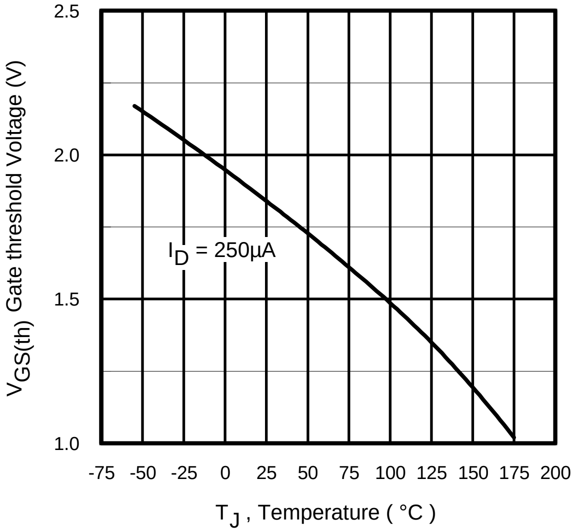
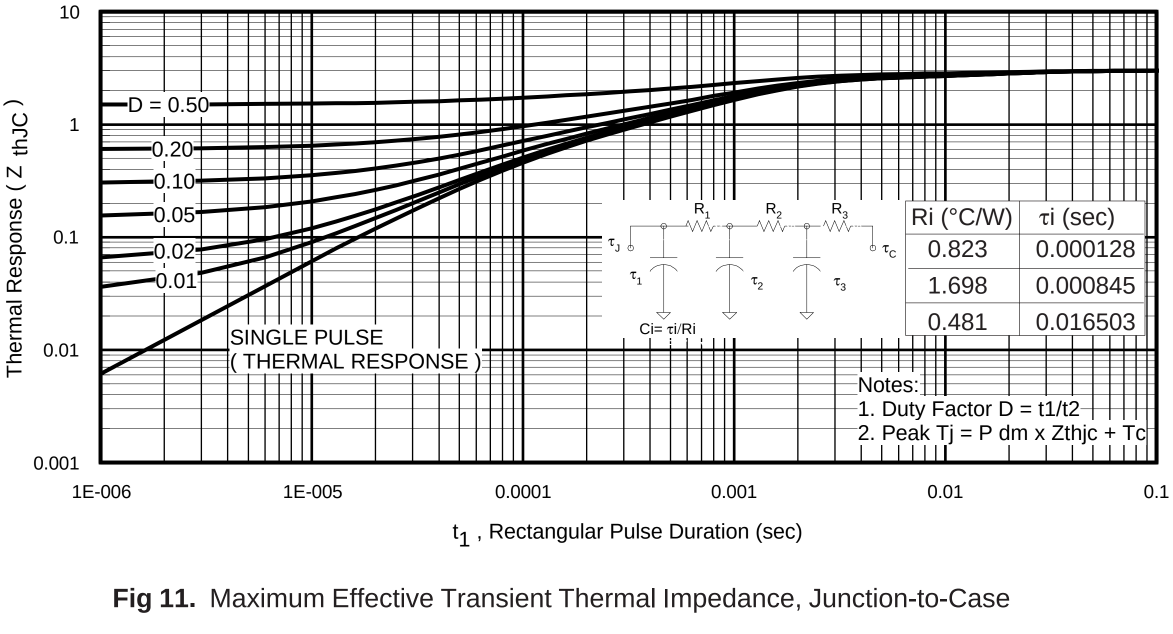


Fig 10. Threshold Voltage vs. Temperature



Ri (°C/W)	τi (sec)
0.823	0.000128
1.698	0.000845
0.481	0.016503

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

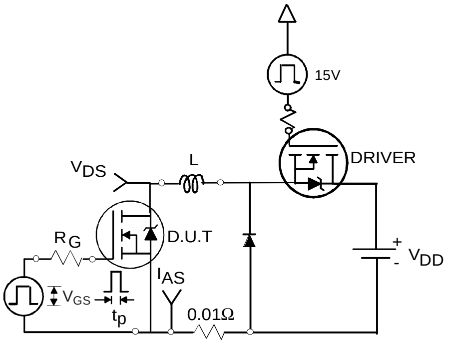


Fig 12a. Unclamped Inductive Test Circuit

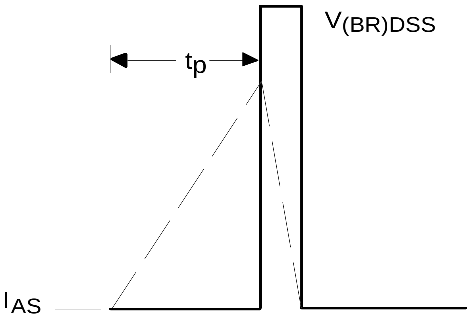


Fig 12b. Unclamped Inductive Waveforms

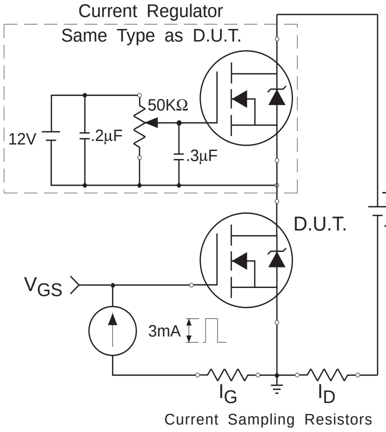


Fig 13. Gate Charge Test Circuit

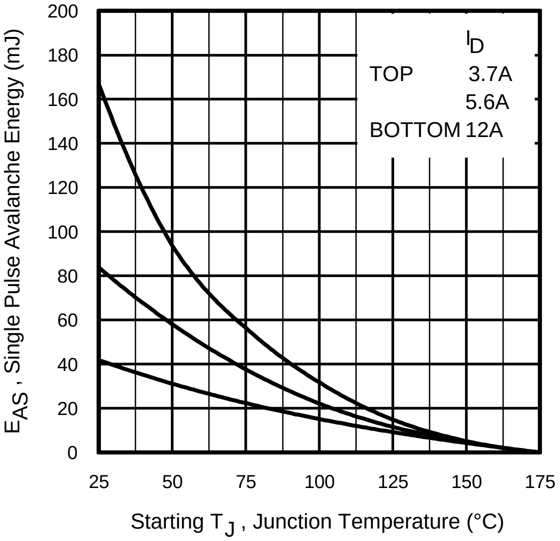


Fig 12c. Maximum Avalanche Energy vs. Drain Current

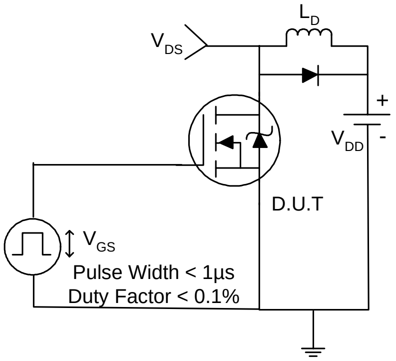


Fig 14a. Switching Time Test Circuit

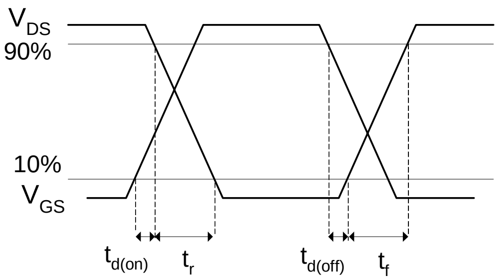


Fig 14b. Switching Time Waveforms

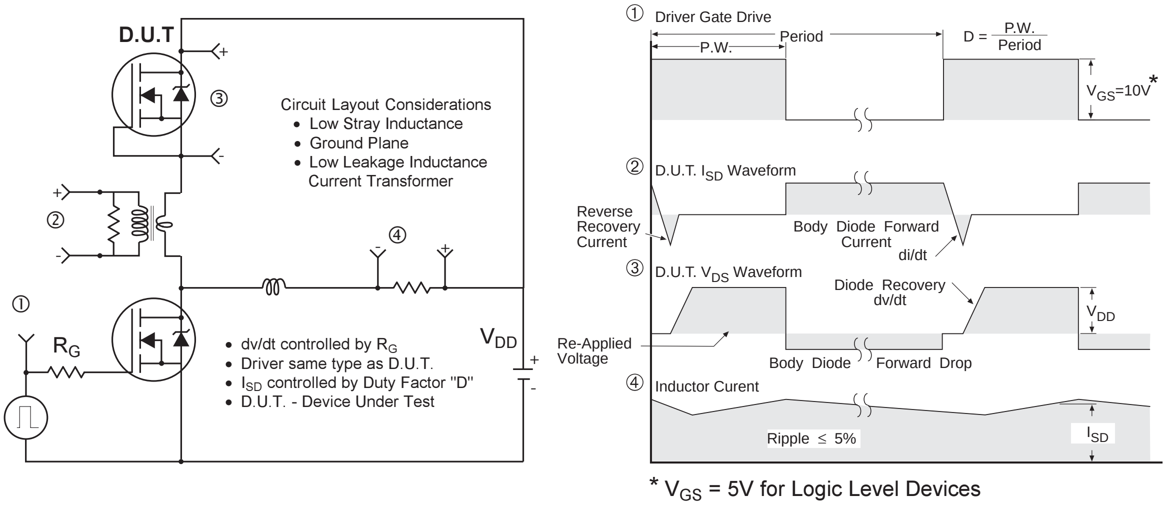


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

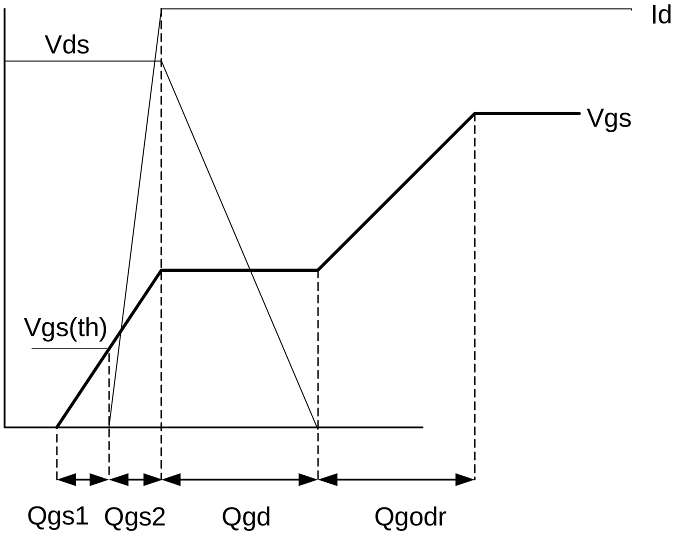


Fig 16. Gate Charge Waveform

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$\begin{aligned} P_{loss} &= \left(I_{rms}{}^{2} \times R_{ds(on)}\right) \\ &+ \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right) \\ &+ \left(Q_g \times V_g \times f\right) \\ &+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) \end{aligned}$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^{*}$$

$$\begin{aligned} P_{loss} &= \left(I_{rms}{}^{2} \times R_{ds(on)}\right) \\ &+ \left(Q_g \times V_g \times f\right) \\ &+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right) \end{aligned}$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

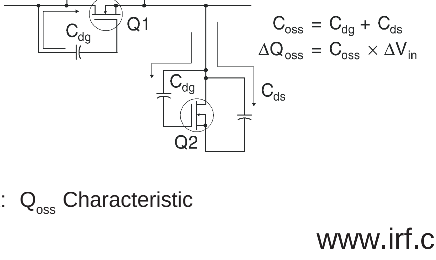
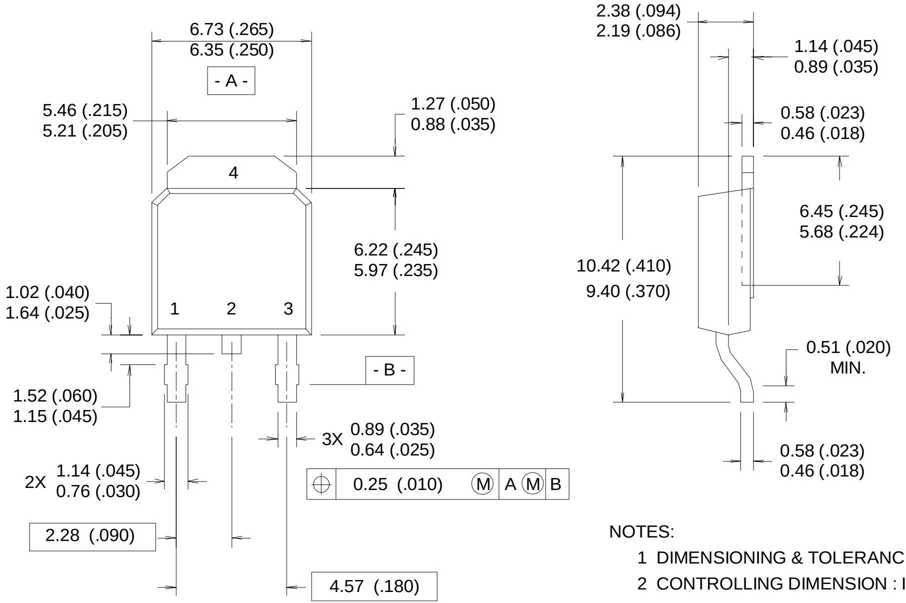


Figure A: Q_{oss} Characteristic

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

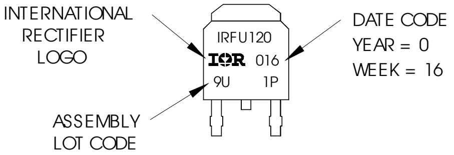
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP,
SOLDER DIP MAX. +0.16 (.006).

D-Pak (TO-252AA) Part Marking Information

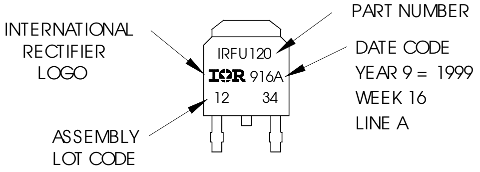
Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P



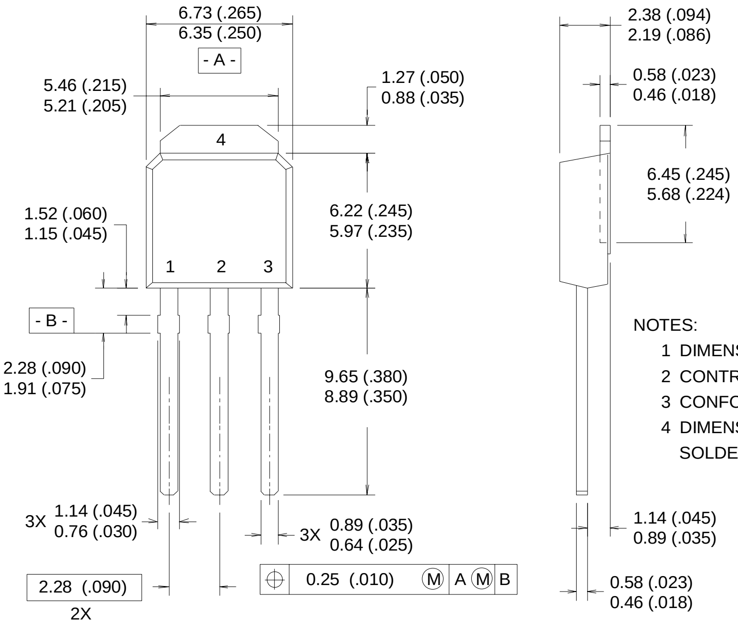
Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

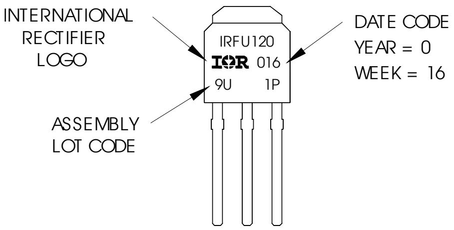
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION : INCH.
3. CONFORMS TO JEDEC OUTLINE TO-252AA.
4. DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

I-Pak (TO-251AA) Part Marking Information

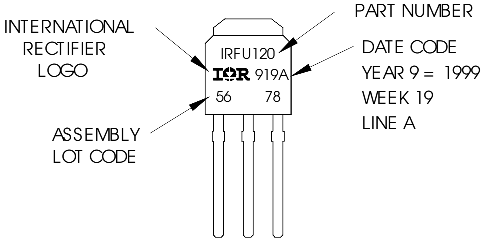
Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P



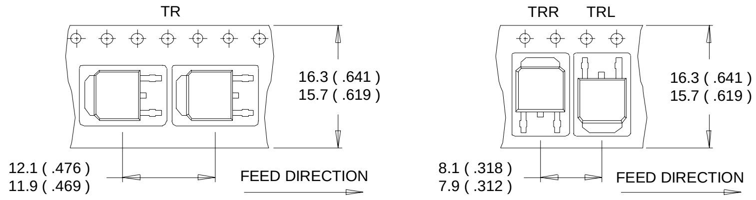
Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

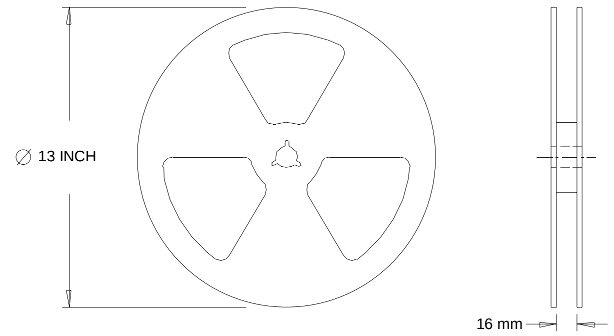


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$, $L = 0.58mH$, $R_G = 25\Omega$, $I_{AS} = 12A$.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.

⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR’s Web site.

International
IOR Rectifier

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TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information**.** 03/03

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/