PIC16(L)F1946/1947

PIC16(L)F1946/1947 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F1946/1947 family devices that you have received conform functionally to the current Device Data Sheet (DS41414**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1946/1947 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A6**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1946/1947 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>(1), (2)					
	DEV<8:0>	Revision ID for Silicon Revision				
		A2	A3	A4	A5	A6
PIC16F1946	10 0101 000	0 0010	0 0011	0 0100	0 0101	0 0110
PIC16LF1946	10 0101 100	0 0010	0 0011	0 0100	0 0101	0 0110
PIC16F1947	10 0101 001	0 0010	0 0011	0 0100	0 0101	0 0110
PIC16LF1947	10 0101 101	0 0010	0 0011	0 0100	0 0101	0 0110

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC16F193X/LF193X/PIC16F194X/LF194X/PIC16LF190X Memory Programming Specification"* (DS41397) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)				
				A2	A3	A4	A5	A6
Oscillator	HS Oscillator	1.1	HS Oscillator min. VDD.	X				
Oscillator	Clock Switching	1.2	Clock switching can cause a single corrupted instruction.	X	X	X	X	
Oscillator	Oscillator Start-up Timer (OST) bit	1.3	OST bit remains set.	X	X	X	X	
ADC	Analog-to-Digital Converter	2.1	ADC conversion does not complete.	X				
Brown-out Reset (BOR)	Brown-out Reset	3.1	BOR set without going below BOR level.	X	X	X	X	
Brown-out Reset (BOR)	Wake-up from Sleep	3.2	Device resets on wake-up from Sleep (Affects LF devices only).	X	X	X	X	
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	4.1	PWM 0% duty cycle direction change.	X				
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	4.2	PWM 0% duty cycle port steering.	X				
Enhanced Universal Synchronous Asynchronous Receiver (EUSART)	Auto-Baud Detect	5.1	Auto-Baud Detect may store incorrect count value in the SPBRG registers.	X	X	X		
MSSP (Master Synchronous Serial Port)	SPI Master mode	6.1	Buffer Full (BF) bit or MSSP Interrupt Flag (SSPIF) bit becomes set half SCK cycle too early.	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6**).

1. Module: Oscillator

1.1 HS Oscillator

The HS oscillator requires a minimum voltage of 3.0 volts (at 65°C or less) to operate at 20 MHz.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X							

1.2 Clock Switching

When switching clock sources between INTOSC clock source and an external clock source, one corrupted instruction may be executed after the switch occurs.

This issue affects Two-Speed Start-Up and Fail-Safe Clock Monitor operation.

Work around

When switching from an external oscillator clock source, first switch to 16 MHz HFINTOSC. Once running at 16 MHz HFINTOSC, configure IRCF to run at desired internal oscillator frequency.

When clock switching from an INTOSC to an external oscillator clock source, first switch from the desired INTOSC frequency to HFINTOSC High-Power mode (8 MHz or 16 MHz). Once running from HFINTOSC, switch to the external oscillator clock source.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X				

1.3 Oscillator Start-up Timer (OST) bit

During the Two-Speed Start-up sequence, the OST is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as the primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer (OST) failing to restart:

- $\overline{\text{MCLR}}$ Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators which take longer than the clock failure time-out period to start.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X				

2. Module: ADC

2.1 Analog-to-Digital Converter (ADC)

Under certain device operating conditions, the ADC conversion may not complete properly. When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the ADGO/DONE bit does not get cleared and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

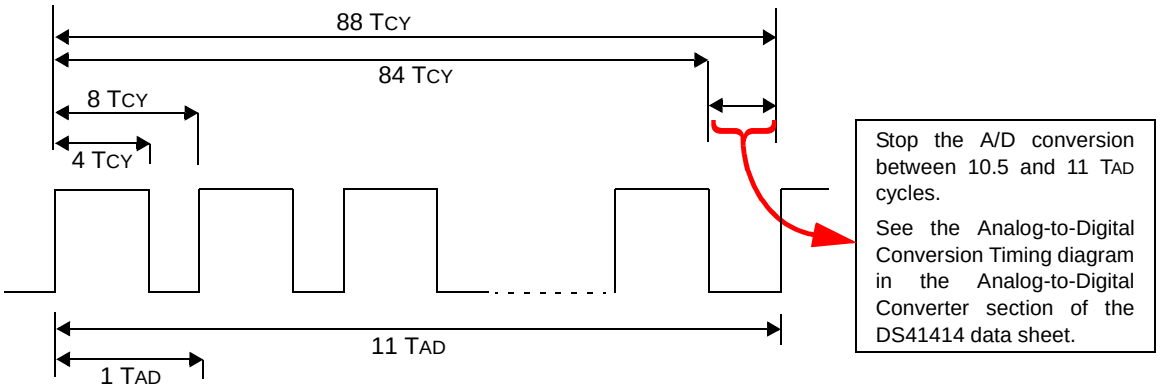
Work around

Method 1: Select the dedicated RC oscillator as the ADC conversion clock source, and perform all conversions with the device in Sleep.

Method 2: Provide a fixed delay in software to stop the A-to-D conversion manually, after all ten bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/DONE bit in software. The GO/DONE bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to Figure 1 for details.

FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE

FOSC = 32 MHz
TCY = 4/32 MHz = 125 nsec
TAD = 1 µsec, ADCS = FOSC/32



See the ADC Clock Period (TAD) vs. Device Operating Frequencies table, in the Analog-to-Digital Converter section of the DS41414 data sheet.

In Figure 1, 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of eight TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

Note:	The exact delay time will depend on the choice of FOSC and the TAD divisor (ADCS) selection. The TCY counts shown in the timing diagram above apply to this example only. Refer to Table 3 for the required delay counts for other configurations.

EXAMPLE 1: CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF     ADCON0, ADGO    ; Start ADC conversion
                        ; Provide 86
                          instruction cycle
                          delay here
BCF     ADCON0, ADGO    ; Terminate the
                          conversion manually
MOVF    ADRESH, W       ; Read conversion
                          result
```

For other combinations of FOSC, TAD values and Instruction cycle delay counts, refer to Table 3.

TABLE 3: INSTRUCTION CYCLE DELAY COUNTS FOR OTHER FOSC AND TAD COMBINATIONS

FOSC	TAD	Instruction Cycle Delay Counts
32 MHz	FOSC/64	172
	FOSC/32	86
16 MHz	FOSC/64	172
	FOSC/32	86
	FOSC/16	43
8 MHz	FOSC/32	86
	FOSC/16	43

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X							

3. Module: Brown-out Reset (BOR)

3.1 Brown-out Reset

If $\overline{MCLR}$ is used to wake the device, while the BOR is set to Sleep and the part is in Sleep, the BOR bit of the PCON register will be cleared without VDD dropping below the BOR level.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X				

3.2 Brown-out Reset

This issue affects only the PIC16LF1946/1947 devices. The device may undergo a BOR Reset when waking up from Sleep and BOR is re-enabled. A BOR Reset may also occur the moment the software BOR is enabled.

Under certain voltage and temperature conditions, after waking from Sleep, if either BOR_nSLEEP is enabled or the SBODEN is enabled, the device may reset.

Method 1: In applications where BOR use is not critical, turn off the BOR in the Configuration Word.

Method 2: Set the FVREN bit of the FVRCON register. Maintain this bit on at all times.

Method 3: When the BOR module is needed only during run-time, use the software-enabled BOR by setting the SBODEN option on the Configuration Word. BOR should be turned off by software before Sleep, then follow the below sequence for turning BOR on after wake-up:

a) Wake-up event occurs;
b) Turn on FVR (FVREN bit of the FVRCON register);
c) Wait until FVRRDY bit is set;
d) Wait 15 µs after the FVR Ready bit is set;
e) Manually turn on the BOR.

Method 4: Use the software-enabled BOR as described in Method 3, but use the following sequence:

a) Switch to internal 32 kHz oscillator immediately before Sleep;
b) Upon wake-up, turn on FVR (FVREN bit of the FVRCON register);
c) Manually turn on the BOR;
d) Switch the clock back to the preferred clock source.

Note: When using the software BOR, follow the steps in Methods 3 or 4 above when enabling BOR for the first time during program execution.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X				

4. Module: Enhanced Capture Compare PWM (ECCP)

4.1 Enhanced PWM

When the PWM is configured for Full-Bridge mode and the duty cycle is set to 0%, writing the PxM<1:0> bits to change the direction has no effect on PxA and PxC outputs.

Work around

Increase the duty cycle to a value greater than 0% before changing directions.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X							

4.2 Enhanced PWM

In PWM mode, when the duty cycle is set to 0% and the STRxSYNC bit is set, writing the STRxA, STRxB, STRxC and the STRxD bits to enable/disable steering to port pins has no effect on the outputs.

Work around

Increase the duty cycle to a value greater than 0% before enabling/disabling steering to port pins.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X							

5. Module: Enhanced Universal Synchronous Asynchronous Receiver (EUSART)

5.1 Auto-Baud Detect

When using automatic baud detection (ABDEN), on occasion, an incorrect count value can be stored at the end of Auto-Baud detection in the SPBRGH:SPBRGL (SPBRG) registers. The SPBRG value may be off by several counts. This condition happens sporadically when the device clock frequency drifts to a frequency where the SPBRG value oscillates between two different values. The issue is present regardless of the baud rate Configuration bit settings.

Work around

When using auto-baud, it is a good practice to always verify the obtained value of SPBRG to ensure it remains within the application specifications. Two recommended methods are shown below.

For additional auto-baud information, see Technical Brief TB3069*, "Use of Auto-Baud for Reception of LIN Serial Communications Devices: Mid-Range and Enhanced Mid-Range"*.

EXAMPLE 2: METHOD 1 – EUSART AUTO-BAUD DETECT WORK AROUND

In firmware, define default, minimum and maximum auto-baud (SPBRG) values according to the application requirements.

For example, if the application runs at 9600 baud at 16 MHz then, the default SPBRG value would be (assuming 16-bit/ Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a +/-5% tolerance is required, so tolerance is 0x67 * 5% = 0x05.

```
#define SPBRG_16BIT   *((*int)&SPBRG;                // define location for 16-bit SPBRG value

const int DEFAULT_BAUD = 0x0067;                     // Default Auto-Baud value
const int TOL = 0x05;                                // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL;             // Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL;             // Maximum Auto-Baud Limit
   •
   •
   •
ABDEN = 1;                                           // Start Auto-Baud
while (ABDEN);                                       // Wait until Auto-Baud completes

if((SPBRG_16BIT > MAX_BAUD)||(SPBRG_16BIT < MIN_BAUD))
{                                                    // Compare if value is within limits
    SPBRG_16BIT = DEFAULT_BAUD);                     // if out of spec, use DEFAULT_BAUD
}
   •                                                // if in spec, continue using the
   •                                                // Auto-Baud value in SPBRG
   •
```

EXAMPLE 3: METHOD 2 – EUSART AUTO-BAUD DETECT WORK AROUND

Similar to Method 1, define default, minimum and maximum auto-baud (SPBRG) values. In firmware, compute a running average of SPBRG. If the new SPBRG value falls outside the minimum or maximum limits, then use the current running average value (Average_Baud), otherwise use the auto-baud SPBRG value and calculate a new running average.

For example, if the application runs at 9600 baud at 16 MHz then, the default SPBRG value would be (assuming 16-bit/ Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a +/-5% tolerance is required, so tolerance is 0x67 * 5% = 0x05.

```
#define SPBRG_16BIT   *((*int)&SPBRG;                // define location for 16-bit SPBRG value

const int DEFAULT_BAUD = 0x0067;                     // Default Auto-Baud value
const int TOL = 0x05;                                // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL;             // Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL;             // Maximum Auto-Baud Limit

int Average_Baud;                                    // Define Average_Baud variable
int Integrator;                                      // Define Integrator variable
   •
   •
   •
Average_Baud = DEFAULT_BAUD;                         // Set initial average Baud rate
Integrator = DEFAULT_BAUD*15;                        // The running 16 count average
   •
   •
   •
ABDEN = 1;                                           // Start Auto-Baud
while (ABDEN);                                       // Wait until Auto-Baud completes

Integrator+ = SPBRG_16BIT;
Average_Baud = Integrator/16;
if((SPBRG_16BIT > MAX_BAUD)||(SPBRG_16BIT < MIN_BAUD))
{                                                    // Check if value is within limits
    SPBRG_16BIT = Average_Baud;                      // If out of spec, use previous average
}
else                                                 // If in spec, calculate the running
{                                                    // average but continue using the
    Integrator+ = SPBRG_16BIT;                       // Auto-Baud value in SPBRG
    Average_Baud = Integrator/16;
    Integrator- = Average_Baud;
}
   •
   •
   •
```

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X					

6. Module: MSSP (Master Synchronous Serial Port)

6.1 SPI Master mode

When the MSSP is used in SPI Master mode and the CKE bit is clear (CKE = 0), the Buffer Full (BF) bit and the MSSP Interrupt Flag (SSPIF) bit becomes set half an SCK cycle early. If the user software immediately reacts to either of the bits being set, a write collision may occur as indicated by the WCOL bit being set.

Work around

To avoid a write collision one of the following methods should be used:

Method 1: Add a software delay of one SCK period after detecting the completed transfer (the BF bit or SSPIF bit becomes set) and prior to writing to the SSPBUF register. Verify the WCOL bit is clear after writing to SSPBUF. If the WCOL bit is set, clear the bit in software and rewrite the SSPBUF register.

Method 2: As part of the MSSP initialization procedure, set the CKE bit (CKE = 1).

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41414**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (4/2010)

Initial release of this document.

Rev B Document (9/2010)

Updated errata to new format; Added Silicon Revision A3.

Rev C Document (12/2010)

Updated errata to add Silicon Revision A4.

Rev D Document (02/2012)

Added Silicon Revision A5; Added Oscillator errata issues 1.2, 1.3 and 1.4; Added Module 5.

Rev E Document (06/2012)

Added MPLAB X IDE; Updated the Affected Silicon Revisions tables in Modules 1.2 and 1.3. Added Module 3.2.

Rev F Document (12/2012)

Added Silicon Revision A6. Updated the Silicon DEVREV values in Table 1 and Silicon Issue Summary in Table 2.

Rev G Document (11/2014)

Added Module 6, MSSP; Other minor corrections.

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