ROHM GROUP
LAPIS SEMICONDUCTOR

FEDL620Q130-01
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ML620Q131/2/3/4/5/6

16-bit micro controller

GENERAL DESCRIPTION

This LSI is a high performance CMOS 16-bit microcontroller equipped with an 16-bit CPU nX-U16/100 and integrated with rich peripheral functions such as the timer, PWM, comparator, voltage level supervisor, UART, I2C, and successive approximation type A/D converter.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by 3-stage pipeline architecture parallel processing. It has the data flash memory area which can be written by software.
In addition, the on-chip debug function that is installed enables software debugging and programming.

FEATURES

- CPU
  - 16-bit RISC CPU (CPU name: nX-U16/100)
  - Instruction system: 16-bit length instruction
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-chip debug function built in
  - Minimum instruction execution time
    30.5 µs (at 32.768 KHz system clock)
    0.063 µs (at 16 MHz system clock)

- Internal memory
  - Flash memory (program area) Rewrite count 100 cycles
    ML620Q131: 8 Kbyte (4K x 16 bits)
    ML620Q132: 16 Kbyte (8K x 16 bits)
    ML620Q133: 24 Kbyte (12K x 16 bits)
    ML620Q134: 8 Kbyte (4K x 16 bits)
    ML620Q135: 16 Kbyte (8K x 16 bits)
    ML620Q136: 24 Kbyte (12K x 16 bits)
  - Flash memory (data area) Rewrite count 10,000 cycles
    2 Kbyte (1K x 16 bits)
  - SRAM
    2 Kbyte (2K x 8 bits)

- Interrupt controller
  - Non-maskable interrupt source: 2 (Internal sources: BACK-UP CLOCK, WDT)
  - Maskable interrupt sources: 30 (Internal sources: 25, External sources: 5)
  - Four interrupt levels and masking function

- Time base counter
  - Low-speed time base counter × 1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
    (The first overflow generates an interrupt, and the second overflow generates a reset)
  - Free running
  - Overflow period: 4 types selectable (125 ms, 500 ms, 2 s, and 8 s at 32.768 kHz)

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- Timers
  - 8 bits x 10 ch (16-bit configuration available)
  - Continuous timer mode/one-shot timer mode
  - Timer start/stop function by software/external trigger input

- PWM
  - Resolution 16 bits x 1 ch
  - Continuous PWM mode/one-shot PWM mode
  - PWM start/stop function by software/external trigger input

- Synchronous serial port
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable
  - Operation in the SPI mode 0/3
  - Overflow detection function

- UART
  - Full-duplex communication x 1 ch
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Internal baud rate generator

- I^2C bus interface
  - Master x 1ch
    Standard mode (100 kbit/s) and fast mode (400 kbit/s) are supported
  - Slave x 1ch
    Standard mode (100 kbit/s) and fast mode (400 kbit/s) are supported

- Successive approximation type A/D converter
  - 10-bit A/D converter
  - ML620Q131/ ML620Q132/ ML620Q133 : Input 6 ch
  - ML620Q134/ ML620Q135/ML620Q136 : Input 8 ch

- Analog Comparator
  - Operation voltage range: VDD = 1.8 to 5.5 V
  - Hysteresis width (only comparator 0): 20 mV (Typ.)
  - Interrupts allow edge selection and sampling selection

- DUTY measurement circuit
  - DUTY ratio measurement by inputting PWM signals with frequencies from 2 KHz to 64 KHz
  - DUTY measurement interrupt: 4 types selectable (64 µs, 0.51 ms, 1.09 ms, 2.18 ms)

- General-purpose ports（including secondary functions）
  - Input-only port
    1 ch (including secondary functions, also used by the on-chip debug pin)
  - I/O port
    ML620Q131/ML620Q132/ML620Q133: 10 ch (including secondary functions)
    ML620Q134/ML620Q135/ML620Q136: 14 ch (including secondary functions)

- Reset
  - RESET_N pin reset
  - Reset by power-on detection
  - Reset by the watchdog timer (WDT) overflow
  - Reset by RAM parity error (enable/disable can be selected)
  - Reset by voltage level detection 0 (VLS0) (enable/disable can be selected)
  - Reset by voltage level detection 1 (VLS1) (enable/disable can be selected)
  - Reset by prohibition program address change

- Voltage level detect function
  - 2 ch
  - Threshold voltage: 12 values selectable
  - Interrupt generation or reset generation can be selected

- Clock
  - Low-speed clock
    Internal low-speed RC oscillation (32.768 KHz)
  - High-speed clock
    PLL oscillation @ internal high-speed RC oscillation (32 MHz*1)
    High-speed crystal oscillation (4 MHz)
    PLL oscillation @ high-speed crystal oscillation (32 MHz*1*2)
  - Selection of high-speed clock mode by software
    PLL oscillation @ internal high-speed RC oscillation mode (16 MHz)
    High-speed crystal oscillation mode (4 MHz)
    PLL oscillation @ high-speed crystal oscillation mode (16 MHz)

    *1) 32 MHz can be used only as the PWMC clock.
    The maximum frequency of the system clock is 16 MHz.
    *2) To use the high-speed crystal oscillation and PLL oscillation @ high-speed crystal oscillation, be sure to connect the high-speed crystal (4 MHz).

- Power management
  - HALT mode: Suspends the instruction execution by CPU (peripheral circuits are in operating states)
  - STOP mode: Stops the low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8, or 1/16 of the oscillation clock)
  - Block Control Function: Powers down (reset registers and stop clock supply) the circuits of unused function blocks

- Shipment
  - 16-pin plastic SSOP
    ML620Q131-xxxMB (Works: ML620Q131-NNNMB)
    ML620Q132-xxxMB (Works: ML620Q132-NNNMB)
    ML620Q133-xxxMB (Works: ML620Q133-NNNMB)
    xxx: ROM code number

  - 16-pin WQFN
    ML620Q131-xxxGD (Works: ML620Q131-NNNGD)
    ML620Q132-xxxGD (Works: ML620Q132-NNNGD)
    ML620Q133-xxxGD (Works: ML620Q133-NNNGD)
    xxx: ROM code number

  - 20-pin plastic TSSOP
    ML620Q134-xxxTD (Works: ML620Q134-NNNTD)
    ML620Q135-xxxTD (Works: ML620Q135-NNNTD)
    ML620Q136-xxxTD (Works: ML620Q136-NNNTD)
    xxx: ROM code number

- Guaranteed operating range
  - Operating temperature: -40 to 105 °C
  - Operating voltage: VDD = 1.6 to 5.5 V

The difference of ML620Q130 series is shown below.

Feature	ML620Q131	ML620Q132	ML620Q133	ML620Q134	ML620Q135	ML620Q136
Shipment	16-pin SSOP/ 16-pin WQFN			20-pin TSSOP		
FLASH capacity (Program area)	8 KB	16 KB	24 KB	8 KB	16 KB	24 KB
Number of input channels for successive approximation type A/D converter	6 ch			8 ch		
Number of input-only ports	1 (also used by the on-chip debug pin)			1 (also used by the on-chip debug pin)		
Number of I/O ports	10			14		

BLOCK DIAGRAM

ML620Q131/ML620Q132/ML620Q133 Block Diagram

"*" indicates the secondary, tertiary or quarternary function.

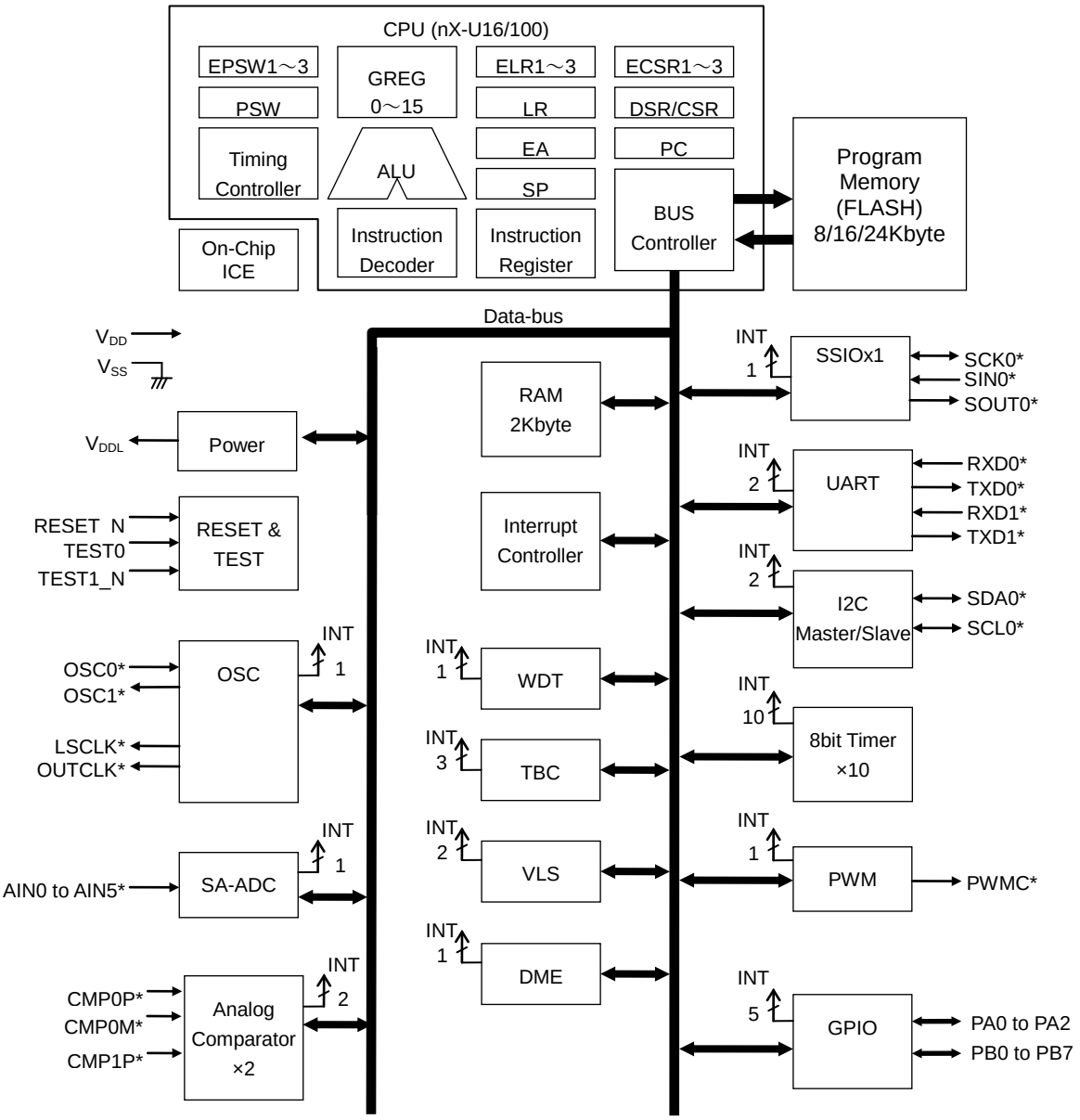


Figure 1-1 ML620Q131/ML620Q132/ML620Q133 Block Diagram

ML620Q134/ML620Q135/ML620Q136 Block Diagram

"*" indicates the secondary, tertiary or quarternary function.

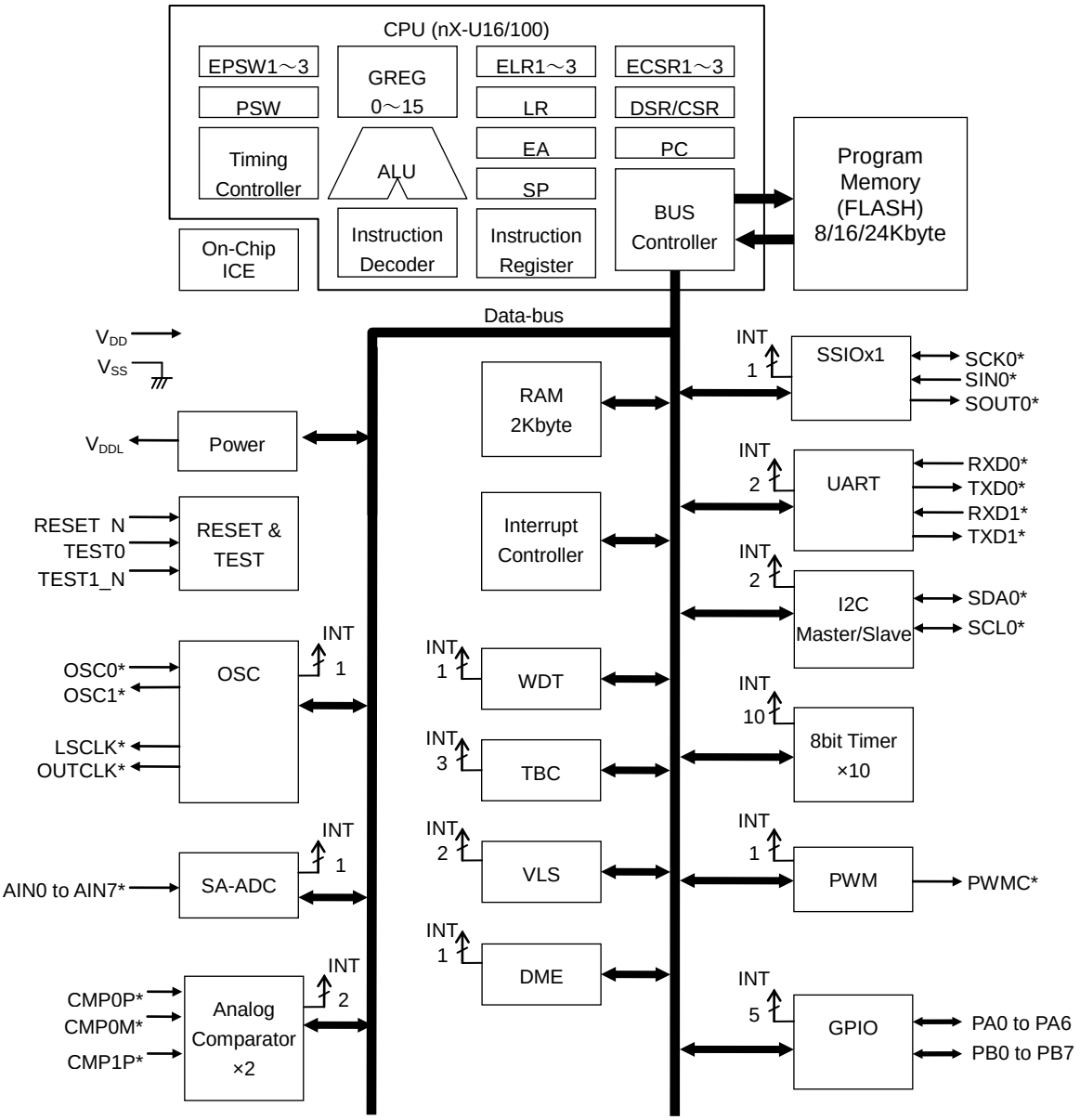


Figure 1-2 ML620Q134/ML620Q135/ML620Q136 Block Diagram

PIN CONFIGURATION

Pin Layout of ML620Q131/ML620Q132/ML620Q133 16pin SSOP Package

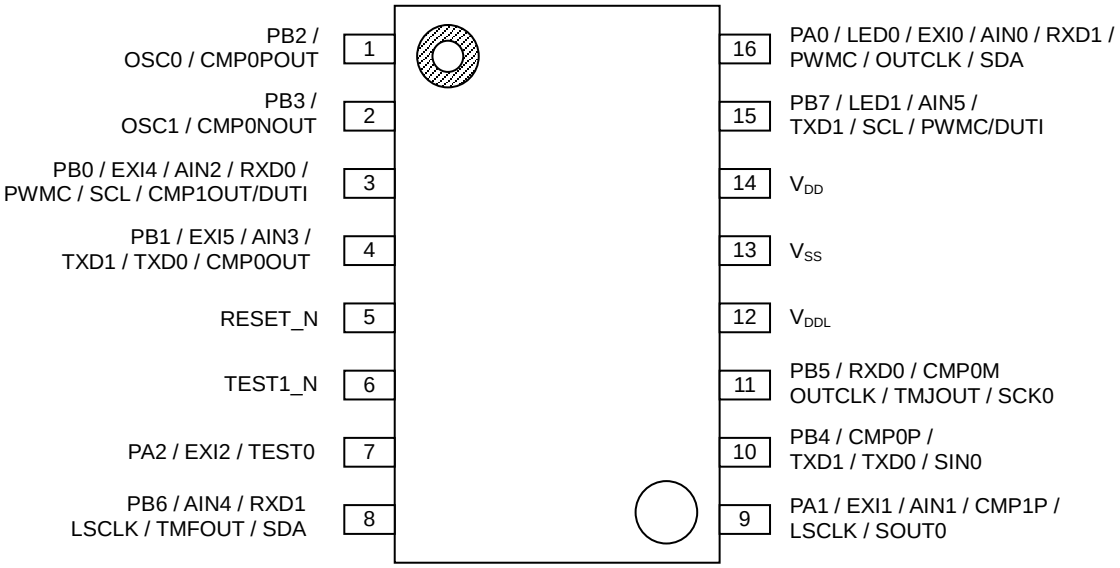


Figure 2 Pin Layout of ML620Q131/ML620Q132/ML620Q133 16pin SSOP Package

Pin Layout of ML620Q131/ML620Q132/ML620Q133 16pin WQFN Package

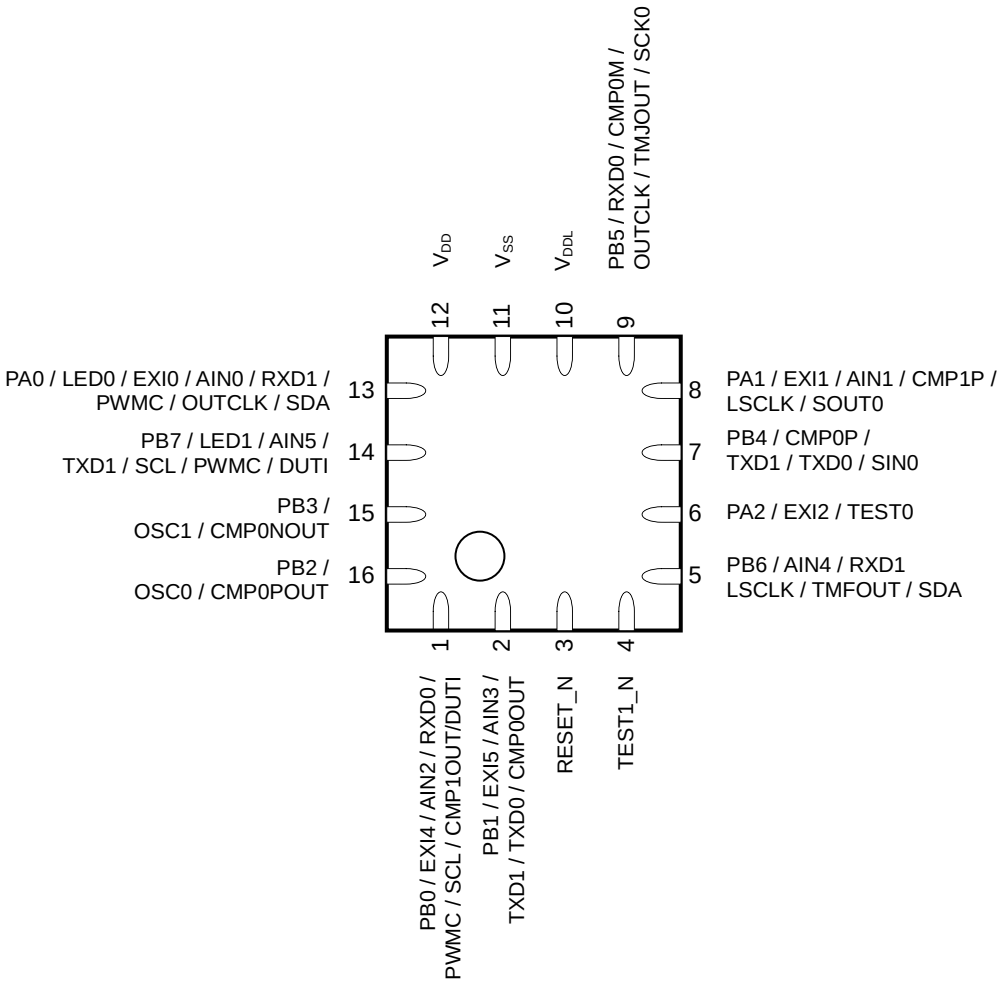


Figure 3 Pin Layout of ML620Q131/ML620Q132/ML620Q133 16pin WQFN Package

Pin Layout of ML620Q134/ML620Q135/ML620Q136 20pin TSSOP Package

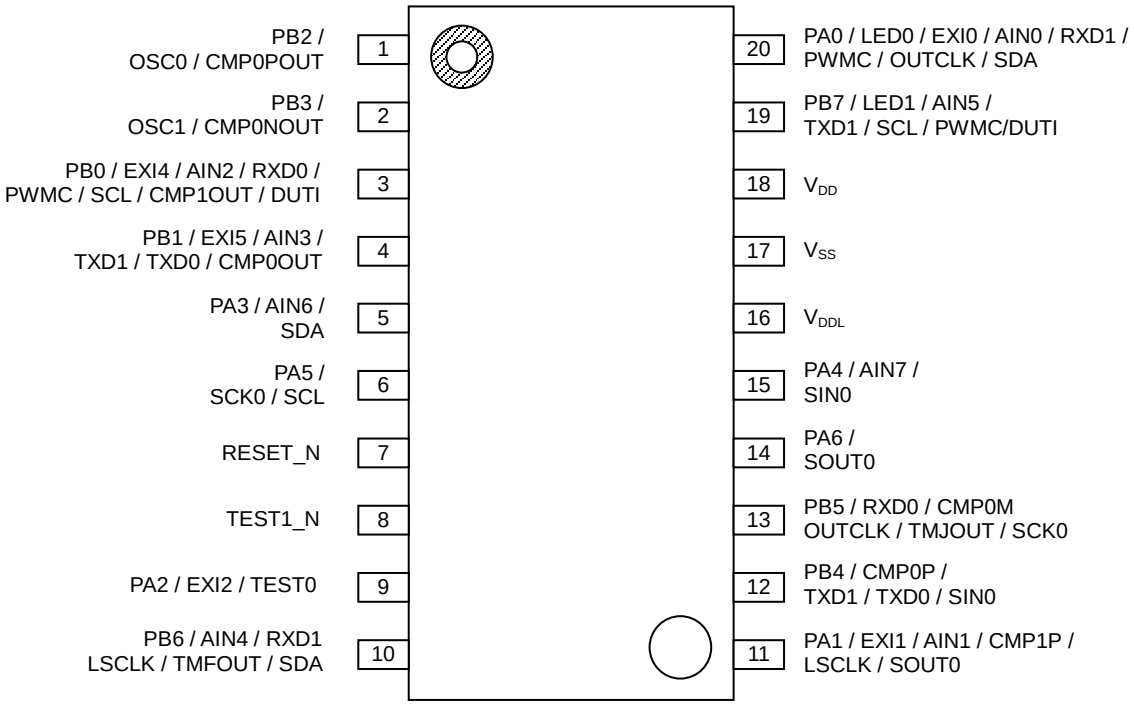


Figure 4 Pin Layout of ML620Q134/ML620Q135/ML620Q136 20pin TSSOP Package

PIN LIST

Table 1 Pin List

PAD No. (16pin SSOP)	PAD No. (16pin WQFN)	PAD No. (20pin TSSOP)	Primary function			Secondary function			Tertiary function			Quartic function		
			Pin name	I/O	Feature	Pin name	I/O	Feature	Pin name	I/O	Feature	Pin name	I/O	Feature
14	12	18	V_{DD}	I/O	Positive power supply pin input/output	—	—	—	—	—	—	—	—	—
12	10	16	V_{DDL}	I/O	Power supply pin for internal logic (Internal generation)	—	—	—	—	—	—	—	—	—
13	11	17	V_{ss}	I/O	Negative power supply pin input/output	—	—	—	—	—	—	—	—	—
5	3	7	RESET_N	I	Reset input pin	—	—	—	—	—	—	—	—	—
6	4	8	TEST1_N	I	Input pin for testing	—	—	—	—	—	—	—	—	—
16	13	20	PA0/ LED0/ EXI0/ AIN0/ RXD1	I/O	I/O port/ LED drive External interrupt 0/ AD input 0/ UART1 reception	PWMC	O	PWMC output	OUTCLK	O	High-speed clock output	SDA	I/O	I^2C data I/O
9	8	11	PA1/ EXI1/ AIN1/ CMP1P	I/O	I/O port/ External interrupt 1/ AD input 1/ Comparator 1 Non-inverting input	—	—	—	LSCLK	O	Low-speed clock output	SOUT0	O	SSIO data output
7	6	9	PA2/ EXI2/ TEST0	I	input port/ External interrupt 2/ Input pin for testing	—	—	—	—	—	—	—	—	—
—	—	5	PA3/ AIN6	I/O	I/O port/ AD input 6	—	—	—	SDA	I/O	I^2C data I/O	—	—	—
—	—	15	PA4/ AIN7	I/O	I/O port/ AD input 7	SIN0	I	SSIO data input	—	—	—	—	—	—
—	—	6	PA5	I/O	I/O port	SCK0	I/O	SSIO clock I/O	SCL	I/O	I^2C clock I/O	—	—	—
—	—	14	PA6	I/O	I/O port	SOUT0	O	SSIO data output	—	—	—	—	—	—
3	1	3	PB0/ EXI4/ AIN2/ RXD0/ DUTI	I/O	I/O port/ External interrupt 4/ AD input 2/ UART0 reception/ DUTY measurement	PWMC	O	PWMC output	SCL	I/O	I^2C clock I/O	CMP1 OUT	O	CMP1 output
4	2	4	PB1/ EXI5/ AIN3	I/O	I/O port/ External interrupt 5/ AD input 3	TXD1	O	UART1 transmission	TXD0	O	UART0 transmission	CMP0 OUT	O	CMP0 output
1	16	1	PB2	I/O	I/O port	OSC0	I	High-speed oscillation	—	—	—	CMP0POUT	O	CMP0P output
2	15	2	PB3	I/O	I/O port	OSC1	O	High-speed oscillation	—	—	—	CMP0NOUT	O	CMP0N output

PAD No. (16pin SSOP)	PAD No. (16pin WQFN)	PAD No. (20pin TSSOP)	Primary function			Secondary function			Tertiary function			Quartic function		
			Pin name	I/O	Feature	Pin name	I/O	Feature	Pin name	I/O	Feature	Pin name	I/O	Feature
10	7	12	PB4/ CMP0P	I/O	I/O port/ Comparator 0 Non-inverting input	TXD1	O	UART1 transmission	TXD0	O	UART0 transmis sion	SIN0	I	SSIO data input
11	9	13	PB5/ RXD0/ CMP0M	I/O	I/O port/ UART0 reception/ Comparator 0 Inverting input	OUTCLK	O	High-speed clock output	TMJ OUT	O	Timer J output	SCK0	I/O	SSIO clock I/O
8	5	10	PB6/ AIN4/ RXD1	I/O	I/O port/ AD input 4/ UART1 reception	LSCLK	O	Low-speed clock output	TMF OUT	O	Timer F output	SDA	I/O	I^2C data I/O
15	14	19	PB7/ LED1/ AIN5/ DUTI	I/O	I/O port/ LED drive AD input 5/ DUTY measurement	TXD1	O	UART1 transmission	SCL	I/O	I^2C clock I/O	PWMC	O	PWMC output

PIN DESCRIPTION

Table 2 Pin Description (1/4)

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quartic	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. The RESET_N pin does not have an internal pull-up resistor.	—	Negative
OSC0	I	Crystal connection pin for the high-speed clock.	Secondary	—
OSC1	O	A crystal oscillator is connected to this pin (4 MHz max.), and capacitors C_{DH} and C_{GH} (see measurement circuit 1) are connected between this pin and V_{SS}. This pin is used as the secondary function of the PB2 and PB3 pins.	Secondary	—
LSCLK	O	Low-speed clock output. This pin is used as the tertiary function of the PA1 pin or the secondary function of the PB6 pin.	Secondary/ Tertiary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the tertiary function of the PA0 pin or the secondary function of the PB5 pin.	Tertiary	—
General-purpose input port				
PA2	I	General-purpose input port.	—	Positive
General-purpose input/output port				
PA0 to PA1 PB0~PB7	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary to quartic functions.	—	Positive
PA3 to PA6	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary to quartic functions. Not available in ML620Q131/ML620Q132/ML620Q133.	—	Positive
Serial (UART)				
TXD0	O	UART0 transmit pin. This pin is used as the tertiary function of the PB1 and PB4 pins.	Tertiary	Positive
TXD1	O	UART1 transmit pin. This pin is used as the secondary function of the PB1, PB4, and PB7 pins.	Secondary	Positive
RXD0	I	UART0 receive pin. This pin is used as the primary function of the PB0 and PB5 pins.	Primary	Positive
RXD1	I	UART1 receive pin. This pin is used as the primary function of the PA0 and PB6 pins.	Primary	Positive
I^2C Bus Interface				
SDA	I/O	NMOS open drain pin for I^2C data input/output. This pin is used as the quartic function of the PA0 pin, the tertiary function of the PA3 pin, or the quartic function of the PB6 pin. A pull-up resistor is connected externally.	Tertiary/ Quartic	Positive
SCL	I/O	NMOS open drain pin for I^2C clock input/output. This pin is used as the tertiary function of the PA5 pin, the tertiary function of the PB0 pin, or the tertiary function of the PB7 pin. A pull-up resistor is connected externally.	Tertiary	Positive

Table 2 Pin Description (2/4)

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quartic	Logic
Synchronous serial (SSIO)				
SIN	I	Synchronous serial data input pin. This pin is used as the secondary function of the PA4 pin or the quartic function of the PB4 pin.	Secondary/ Quartic	Positive
SCK0	I/O	High-speed clock input pin. This pin is used as the secondary function of the PA5 pin or the quartic function of the PB5 pin.	Secondary/ Quartic	—
SOUT0	O	High-speed clock output pin. This pin is used as the quartic function of the PA1 pin or the secondary function of the PA6 pin.	Secondary/ Quartic	Positive
PWM				
PWMC	O	PWMC output pin. This pin is used as the secondary function of the PA0 and PB0 pins or the quartic function of the PB7 pin.	Secondary/ Quartic	Positive/ negative
External interrupt				
EXI0 to 2	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. This pin is used as the primary function of the PA0 to PA2 pins.	Primary	Positive/ negative
EXI4,5	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. This pin is used as the primary function of the PB0 and PB1 pins.	Primary	Positive/ negative
Timer				
TnTG	I	External trigger input pin of the timer 0, timer 1, timer E, timer F, timer G, timer H, timer I, timer J, timer K, or timer L. This pin is used as the primary function of the PA0 to PA2 and PB0 to PB7 pins.	Primary	—
TMJOUT	O	Timer J output pin. This pin is used as the tertiary function of PB5.	Tertiary	Positive
TMFOUT	O	Timer F output pin. This pin is used as the tertiary function of PB6.	Tertiary	Positive
LED drive				
LED0, 1	O	Pins for LED driving. Allocated to the primary function of the PA0 and PB7 pins.	Primary	Positive/ negative

Table 2 Pin Description (3/4)

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quartic	Logic
Successive approximation type A/D converter				
AIN0	I	Ch0 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA0 pin.	Primary	—
AIN1	I	Ch1 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA1 pin.	Primary	—
AIN2	I	Ch2 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB0 pin.	Primary	—
AIN3	I	Ch3 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB1 pin.	Primary	—
AIN4	I	Ch4 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB6 pin.	Primary	—
AIN5	I	Ch5 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB7 pin.	Primary	—
AIN6	I	Ch6 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA3 pin. Not available in ML620Q131/ML620Q132/ML620Q133.	Primary	—
AIN7	I	Ch7 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA4 pin. Not available in ML620Q131/ML620Q132/ML620Q133.	Primary	—
Comparator				
CMP0P	I	Comparator 0 non-inverting input. This pin is used as the primary function of the PB4 pin.	Primary	—
CMP0M	I	Comparator 0 inverting input. This pin is used as the primary function of the PB5 pin.	Primary	—
CMP0OUT	O	Comparator 0 output pin. This pin is used as the quartic function of the PB1 pin.	Quartic	—
CMP0POUT	O	Comparator 0 output pin. This pin is used as the quartic function of the PB2 pin.	Quartic	—
CMP0NOUT	O	Comparator 0 output pin. This pin is used as the quartic function of the PB3 pin.	Quartic	—
CMP1P	I	Comparator 1 non-inverting input. This pin is used as the primary function of the PA1 pin.	Primary	—
CMP1OUT	O	Comparator 1 output pin. This pin is used as the quartic function of the PB0 pin.	Quartic	—
DUTY measurement circuit				
DUTI	I	PWM waveform input for the DUTY measurement circuit. This pin is used as the primary function of the PB0 and PB7 pins.	Primary	—

Table 2 Pin Description (4/4)

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quartic	Logic
For testing				
TEST0	I	Input pin for testing. This pin is used as the primary function of the PA2 pin.	—	Positive
TEST1_N	I	Input pin for testing. A pull-up resistor is internally connected.	—	Negative
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—
V_{DDL}	—	Power supply pin for internal logic (internally generated). Capacitor C_L (see measurement circuit 1) is connected between this pin and V_{SS}.	—	—

TERMINATION OF UNUSED PINS

Table 3 Termination of unused pins

Pin	Recommended pin termination
RESET_N	V_{DD}
TEST1_N	open
PA0 to PA1	open
PA2/TEST0	V_{SS}
PA3 to PA6	open
PB0 to PB7	open

Note:
For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +6.5	V
Power supply voltage 2	V_{DDL}	Ta = 25°C	–0.3 to +2.0	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1 (PA0 to PA1) (PA3 to PA6)* (PB0 to PB7)	I_{OUT1}	Ta = 25°C	–12 to +11	mA
Output current 2 (PA0) (PB7)	I_{OUT2}	Ta = 25°C When N-channel open drain output mode is selected	–12 to +20	mA
Power dissipation	PD	Ta = 25°C	1	W
Storage temperature	T_{STG}	—	–55 to +150	°C

* : ML620Q131/ ML620Q132/ ML620Q133 do not have the peripherals.

Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	–40 to +105	°C
Operating voltage	V_{DD}	—	1.6 to 5.5	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.6 to 5.5V	30k to 32.768k	Hz
		V_{DD} = 1.8 to 5.5V	30k to 16M	
High-speed crystal oscillation frequency	f_{XTH}	V_{DD} = 1.8 to 5.5V	4.0M	Hz
High-speed crystal oscillation external capacitor	C_{DH}	Use NX8045GE (NIHON DEMPA KOGYO CORP.)	16	pF
	C_{GH}		16	
Capacitor externally connected to V_{DDL} pin	C_L	—	2.2±30%	µF

Flash Memory Operating Conditions

(V_{SS} = 0V)

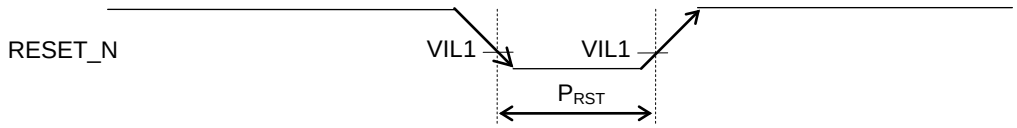
Parameter	Symbol	Condition		Range	Unit
Operating temperature	T_{OP}	Data flash memory, At write/erase		-40 to +105	°C
		Flash ROM, At write/erase		0 to +40	
Operating voltage	V_{DD}	At write/erase		1.6 to 5.5	V
Maximum rewrite count	C_{EPD}	Data Flash		10,000	times
	C_{EPP}	Program Flash		100	
Erase unit	—	Chip erase		All area	—
	—	Block erase	Program Flash	4	KB
			Data Flash	2	KB
	—	Sector erase (Data Flash only)		1	KB
Erase time	—	Chip erase, Block erase, Sector erase		100	ms
Write unit	—	—		1 word (2 Bytes)	—
Write time (Max.)	—	1 word (2 Bytes)		40	µs
Data retention period	Y_{DR}	—		15	years

DC Characteristics Conditions (1/5)

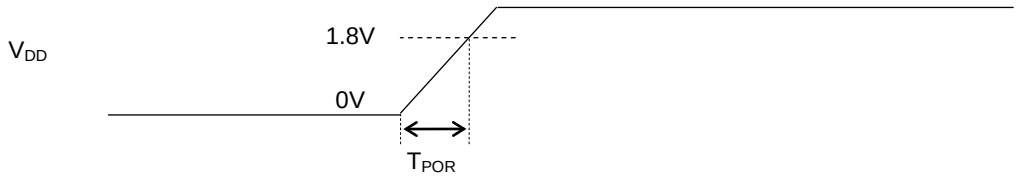
(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Low-speed RC oscillator frequency	f_{RCL}	Ta= +25°C	Typ -1%	32.768k	Typ +1%	Hz	1
		Ta= -40 to 85°C	Typ -2.5%	32.768k	Typ +2.5%	Hz	
		Ta= -40 to 105°C	Typ -3%	32.768k	Typ +3%	Hz	
PLL oscillation frequency*1	f_{PLL}	Ta= -20 to 85°C, V_{DD} = 1.8 to 5.5V	Typ -1%	32	Typ +1%	MHz	
		Ta= -40°C to +105°C, V_{DD} = 1.8 to 5.5V	Typ -1.5%	32	Typ +1.5%	MHz	
Low-speed RC oscillation start time*1	T_{RCL}	—	—	—	65	µs	
High-speed RC oscillation start time*1	T_{RCH}	V_{DD} = 1.8 to 5.5V	—	—	5	µs	
High-speed crystal oscillation start time*1	T_{XTH}	V_{DD} = 1.8 to 5.5V	—	2	20	ms	
PLL oscillation start time	T_{PLL}	V_{DD} = 1.8 to 5.5V	—	—	2	ms	
Reset pulse width	P_{RST}	—	100	—	—	µs	
Reset noise rejection pulse width	P_{NRST}	—	—	—	0.4		
Power On Reset rising time	T_{POR}	—	—	—	10	ms	

*1: 2048 clock average. The CPU clock is max. f_{PLL}/2.
*2: Use 4MHz Crystal Oscillator NX8045GE (NIHON DEMPA KOGYO CORP.)



Reset pulse width (P_{RST})



Power On Reset V_{DD} Rising Time (T_{POR})

DC Characteristics Conditions (2/5)

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
VLS0 threshold voltage	V_{VLS0}	VLS03 to 0 = 00H	Rise	1.64	1.67	1.70	V	1
			Fall	1.60	1.63	1.66		
		VLS03 to 0 = 01H	Rise	1.74	1.77	1.81		
			Fall	1.70	1.73	1.77		
		VLS03 to 0 = 02H	Rise	1.84	1.88	1.91		
			Fall	1.80	1.84	1.87		
		VLS03 to 0 = 03H	Rise	1.94	1.98	2.02		
			Fall	1.90	1.94	1.98		
		VLS03 to 0 = 04H	Rise	2.05	2.09	2.13		
			Fall	2.00	2.04	2.08		
		VLS03 to 0 = 05H	Rise	2.45	2.50	2.55		
			Fall	2.40	2.45	2.50		
		VLS03 to 0 = 06H	Rise	2.56	2.61	2.66		
			Fall	2.50	2.55	2.60		
		VLS03 to 0 = 07H	Rise	2.66	2.71	2.76		
			Fall	2.60	2.65	2.70		
		VLS03 to 0 = 08H	Rise	2.76	2.81	2.87		
			Fall	2.70	2.75	2.81		
		VLS03 to 0 = 09H	Rise	2.86	2.92	2.97		
			Fall	2.80	2.86	2.91		
		VLS03 to 0 = 0AH	Rise	2.96	3.02	3.08		
			Fall	2.90	2.96	3.02		
		VLS03 to 0 = 0BH	Rise	4.01	4.09	4.17		
			Fall	3.90	3.98	4.06		
VLS1 threshold voltage	V_{VLS1}	VLS13 to 0 = 00H		1.60	1.63	1.66		
		VLS13 to 0 = 01H		1.70	1.73	1.77		
		VLS13 to 0 = 02H		1.80	1.84	1.87		
		VLS13 to 0 = 03H		1.90	1.94	1.98		
		VLS13 to 0 = 04H		2.00	2.04	2.08		
		VLS13 to 0 = 05H		2.40	2.45	2.50		
		VLS13 to 0 = 06H		2.50	2.55	2.60		
		VLS13 to 0 = 07H		2.60	2.65	2.70		
		VLS13 to 0 = 08H		2.70	2.75	2.81		
		VLS13 to 0 = 09H		2.80	2.86	2.91		
		VLS13 to 0 = 0AH		2.90	2.96	3.02		
		VLS13 to 0 = 0BH		3.90	3.98	4.06		

DC Characteristics Conditions (3/5)

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Comparator0 same phase input voltage range	V_{CMR}	V_{DD} = 1.8 to 5.5V		0.1	—	V_{DD} -1.5	V	4
Comparator0 Hysteresis	V_{HYSP}	Ta = 25℃, V_{DD} = 5.0V		10	20	30	mV	
		V_{DD} = 5.0V		5	20	35		
Comparator0 input offset	V_{CMOF}	Ta = 25℃, V_{DD} = 5.0V		—	—	7		
Comparator reference voltage error *3	V_{CMREF}	Ta = 25℃ V_{DD} = 1.8 to 5.5V		-25	—	25		
		V_{DD} = 1.8 to 5.5V		-50	—	50		
Supply current 1	IDD1	CPU is in STOP state*1. Low-speed oscillation is stopped. V_{DD}=5.0V	Ta = -40 to +105℃	—	1	22	μA	1
			Ta = -40 to +85℃	—	1	9		
Supply current 2	IDD2	Internal RC Oscillating. CPU is in HALT state (LTBC,WBC: Operating*1). High-speed oscillation is stopped. V_{DD}=3.0V	Ta = -40 to +105℃	—	3.5	26		
Supply current 3	IDD3	CPU: Running at 32kHz*1 High-speed oscillation is stopped. V_{DD}=3.0V	Ta = -40 to +105℃	—	13	42		
Supply current 4	IDD4	CPU: Running at 16MHz PLL oscillating mode used High-speed crystal oscillation *2 VDD=5.0V		—	4.5	5.5	mA	
Supply current 5	IDD5	CPU: Running at 16MHz PLL oscillating mode used High-speed RC oscillation *2 VDD=5.0V		—	4.5	5.5		

*1 : LTBC and WDT is operating, Significant bits of BLKCON0 to BLKCON4 registers are all “1”

*2 : CPU running rate is 100%, min. instruction execution time is approx. 62.5ns@16MHz

*3 : Including comparator input offset voltage

DC Characteristics Conditions (4/5)

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=−40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage 1 (PA0 to PA1) (PA3 to PA6)* (PB0 to PB7)	VOH1	IOH1 = −0.5mA		V_{DD} −0.5	—	—	V	2
	VOL1	IOL1 = +0.5mA		—	—	0.5		
Output voltage 2 (PA0) (PB7)	VOL2	When N-channel open drain output mode is selected	IOL2 = +10mA $V_{DD} \geq 5.0V$	—	—	0.5		
			IOL2 = +8mA $V_{DD} \geq 3.0V$	—	—	0.5		
			IOL3 = +3mA $V_{DD} \geq 2.0V$	—	—	0.4		
			IOL3 = +2mA $2.0V > V_{DD} \geq 1.8V$	—	—	VDD* 0.2		
Output leakage current (PA0 to PA1) (PA3 to PA6)* (PB0 to PB7)	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		−1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}		—	—	1		4
	IIL1	VIL1 = V_{SS}		−1	—	—		
Input current 2 (TEST1_N)	IIH2	VIH2 = V_{DD}		—	—	1		
	IIL2	VIL2 = V_{SS}		−1500	−300	−20		
Input current 3 (PA0 to PA1) (PA2/TEST0) (PA3 to PA6)* (PB0 to PB7)	IIH3	VIH3 = V_{DD} (when pulled down)		2	30	250		
	IIL3	VIL3 = V_{SS} (when pulled up)		−250	−30	−2		
	IIH3Z	VIH3 = V_{DD} (in high-impedance state)		—	—	1		
	IIL3Z	VIL3 = V_{SS} (in high-impedance state)		-1	—	—		

* : ML620Q131/ ML620Q132/ ML620Q133 do not have the peripherals.

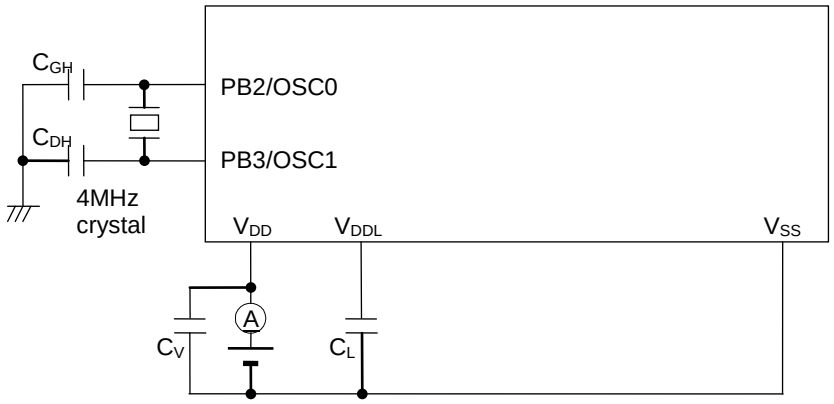
DC Characteristics Conditions (5/5)

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input voltage 1 (RESET_N) (TEST1_N) (PA0 to PA1) (PA2/TEST0) (PA3 to PA6)* (PB0 to PB7)	VIH1	—	0.7× V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3× V_{DD}		
Input pin capacitance (RESET_N) (TEST1_N) (PA0 to PA1) (PA2/TEST0) (PA3 to PA6)* (PB0 to PB7)	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	10	pF	—

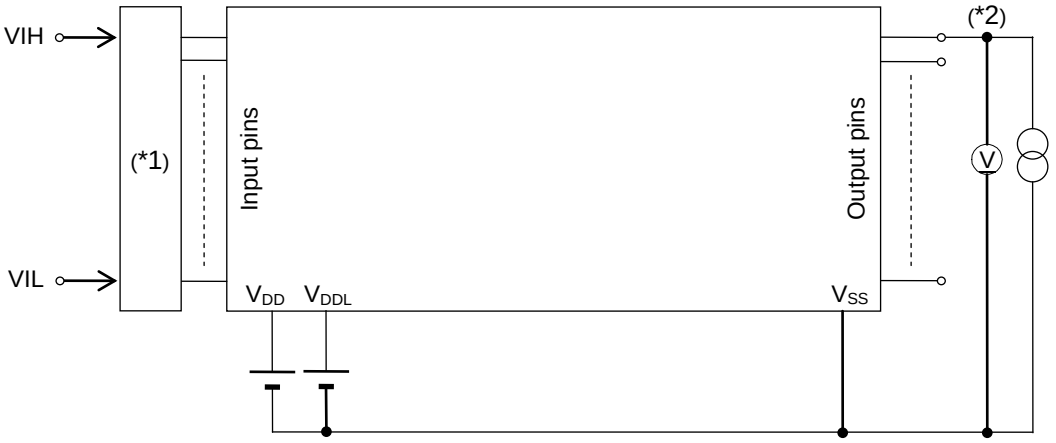
* : ML620Q131/ ML620Q132/ ML620Q133 do not have the peripherals.

Measuring circuit 1



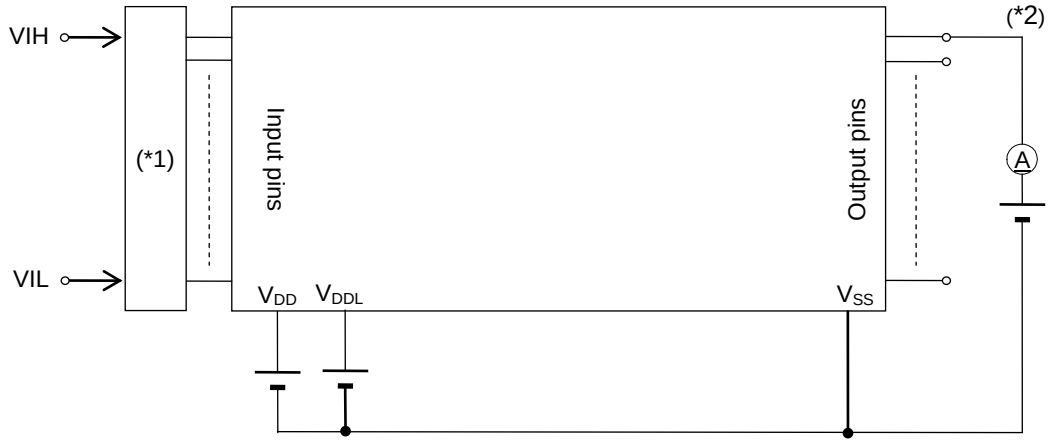
C_V : 2.2µF
C_L : 2.2µF
C_{GH} : 16pF
C_{DH} : 16pF
4MHz crystal : NX8045GE
(NIHON DEMPA KOGYO CORP.)

Measuring circuit 2



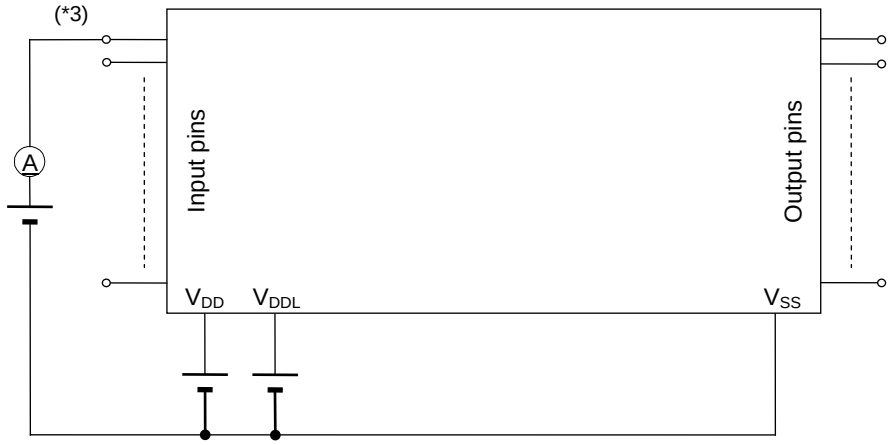
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring circuit 3



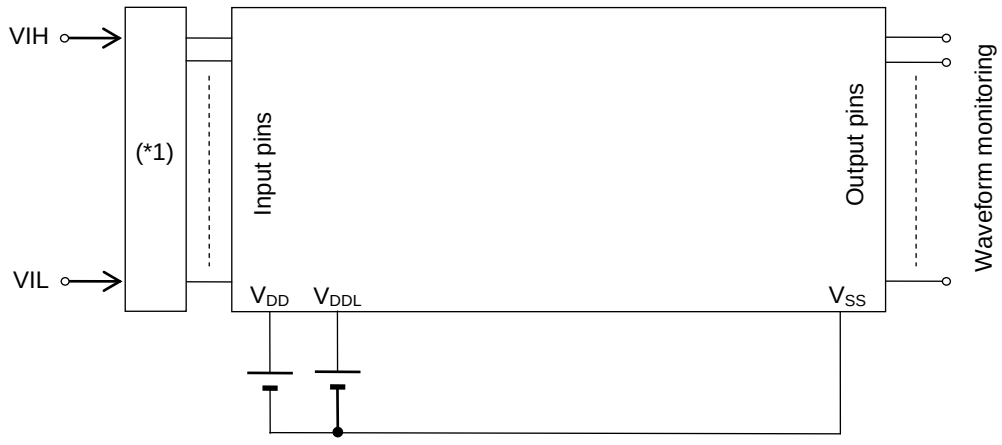
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring circuit 4



*3: Measured at the specified input pins.

Measuring circuit 5

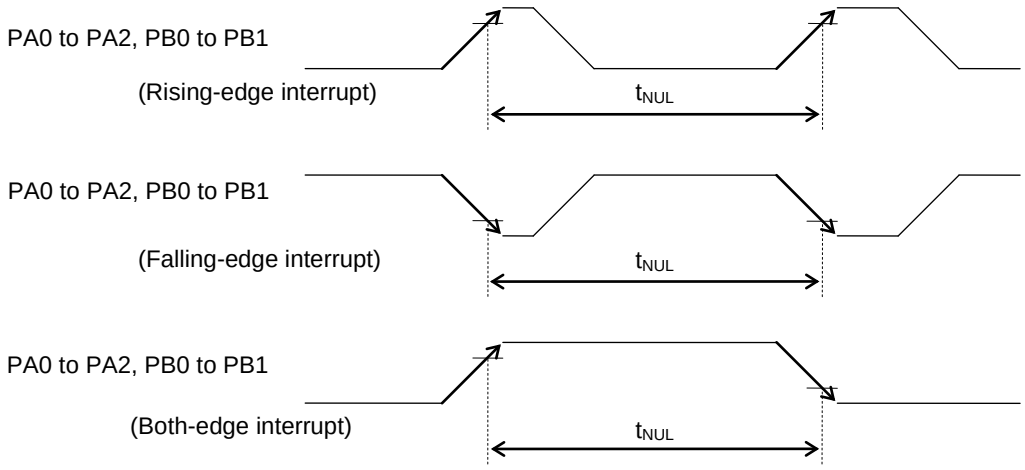


*1: Input logic circuit to determine the specified measuring conditions.

AC Characteristics (External Interrupt)

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU is executing NOP instruction	2.5 × LSCLK	—	3.5 × LSCLK	µs

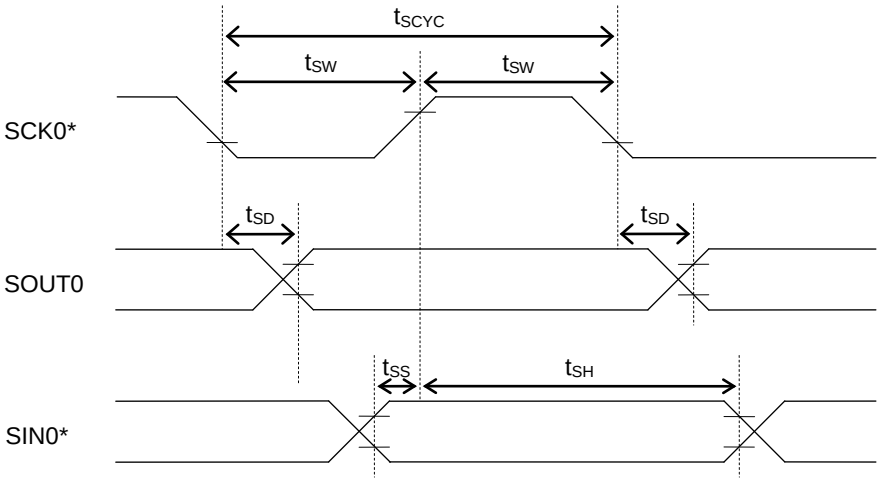


AC Characteristics (Synchronous Serial Port)

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle (slave mode)	t_{SCYC}	—	1	—	—	µs
SCK output cycle (master mode)	t_{SCYC}	—	—	SCK(*1)	—	sec
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation stopped	0.4	—	—	µs
		During high-speed oscillation	200	—	—	ns
SCK output pulse width (master mode)	t_{SW}	—	SCK(*1) ×0.4	SCK(*1) ×0.5	SCK(*1) ×0.6	sec
SOUT output delay time (slave mode)	t_{SD}	—	—	—	360	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	160	ns
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (Master mode)	t_{SS}	—	180	—	—	ns
SIN input hold time	t_{SH}	—	80	—	—	ns

*1: Clock period selected by S0CK3–0 of the serial port n mode register (SIO0MOD1)



*: Indicates the secondary function of the corresponding port.

AC Characteristics (I2C Bus Interface: Standard Mode 100kHz)

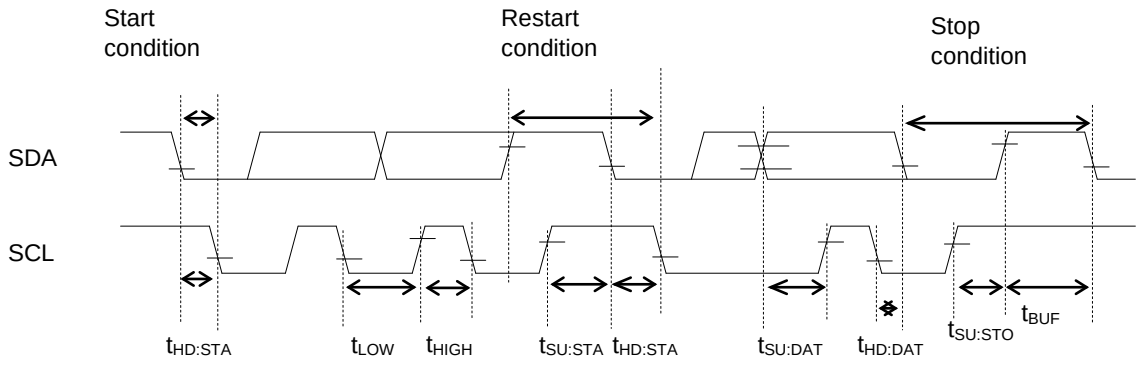
(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

AC Characteristics (I2C Bus Interface: Fast Mode 400kHz)

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL "L" level time	t_{LOW}	—	1.3	—	—	µs
SCL "H" level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs

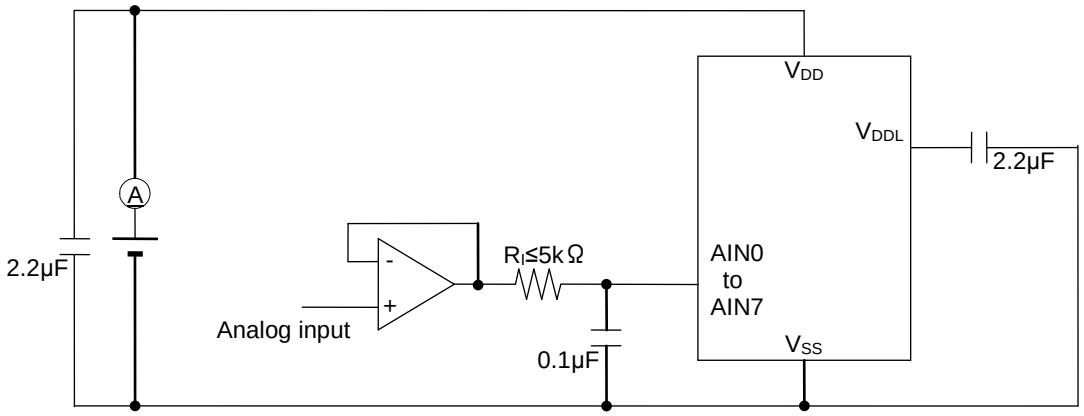


Note:
Current drive ability of PA3, PA5, PB0 and PB6 in N-ch open drain mode is lower than that of PA0 and PB7.
Therefore, the fast mode (400kbps) cannot be available when PA5 or PB0 is set as SCL function and when PA3 or PB6 is set as SDA function.
For more details, see the characteristics of VOL1 and VOL2 in DC Characteristics Conditions (4/5).

Successive Approximation Type A/D Converter

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=−40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	—	—	—	10	bits
Integral non-linearity error	INL	2.7V ≤ V_{DD} ≤ 5.5V	−4	—	+4	LSB
		2.2V ≤ V_{DD} < 2.7V	−6	—	+6	
		1.8V ≤ V_{DD} < 2.2V	−10	—	+10	
Differential non-linearity error	DNL	2.7V ≤ V_{DD} ≤ 5.5V	−3	—	+3	
		2.2V ≤ V_{DD} < 2.7V	−5	—	+5	
		1.8V ≤ V_{DD} < 2.2V	−9	—	+9	
Zero-scale error	V_{OFF}	RI ≤ 5kΩ	−6	—	+6	
Full-scale error	FSE	RI ≤ 5kΩ	−6	—	+6	
Input impedance	R_I	—	—	—	5k	Ω
A/D operating voltage	V_{DD}	—	1.8	—	5.5	V
Conversion time	t_{CONV}	CPU works in PLL oscillation mode SACK bit = 0 2.7V ≤ V_{DD} ≤ 5.5V	—	13.67	—	µs
		CPU works in PLL oscillation mode SACK bit = 1 1.8V ≤ V_{DD} ≤ 5.5V	—	41.26	—	

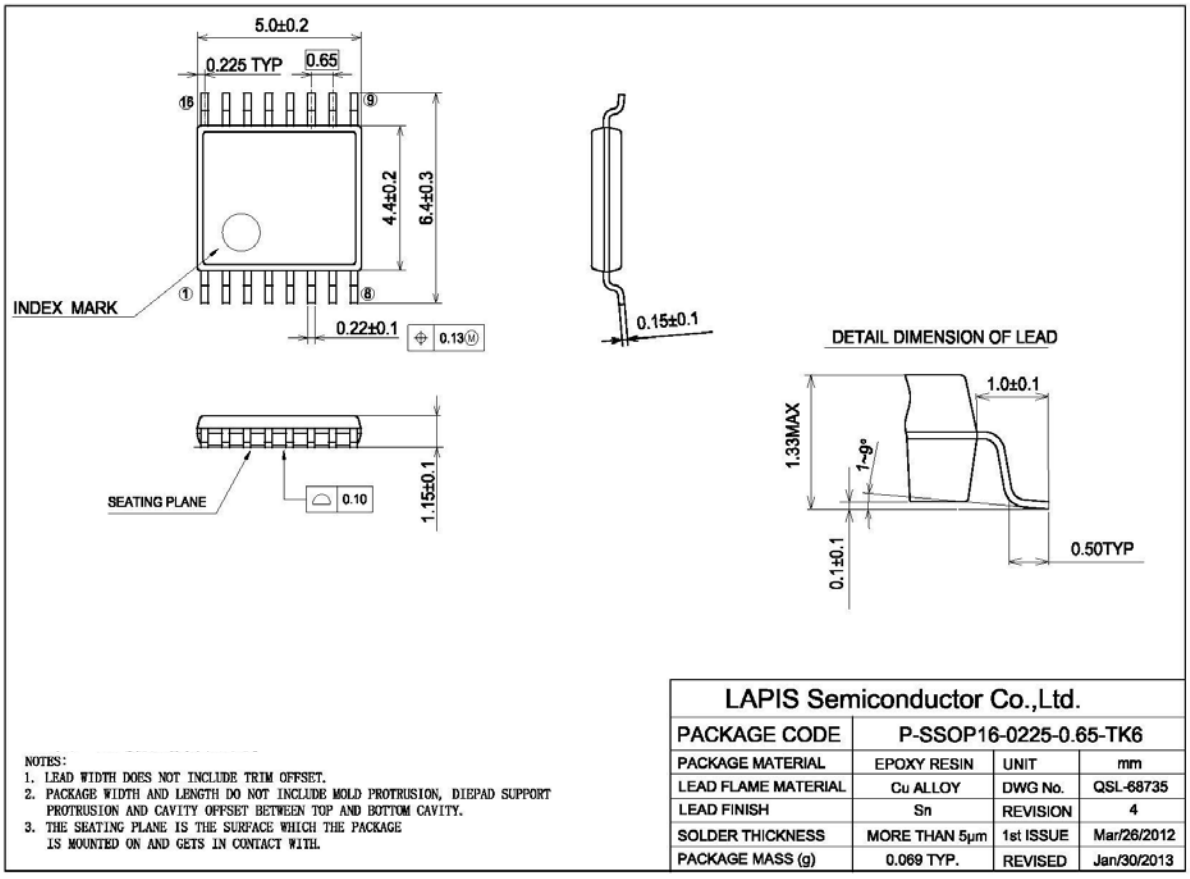


PACKAGE DIMENSIONS

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact LAPIS SEMICONDUCTOR's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

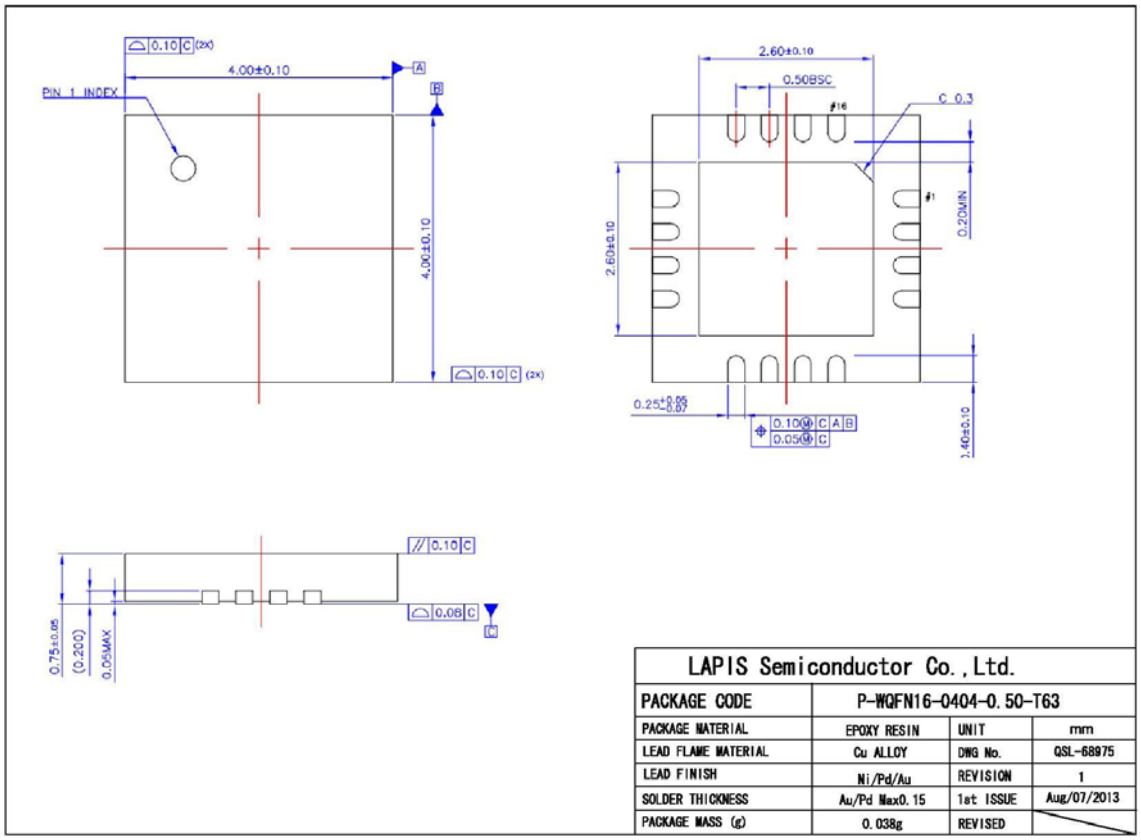
16pin SSOP



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

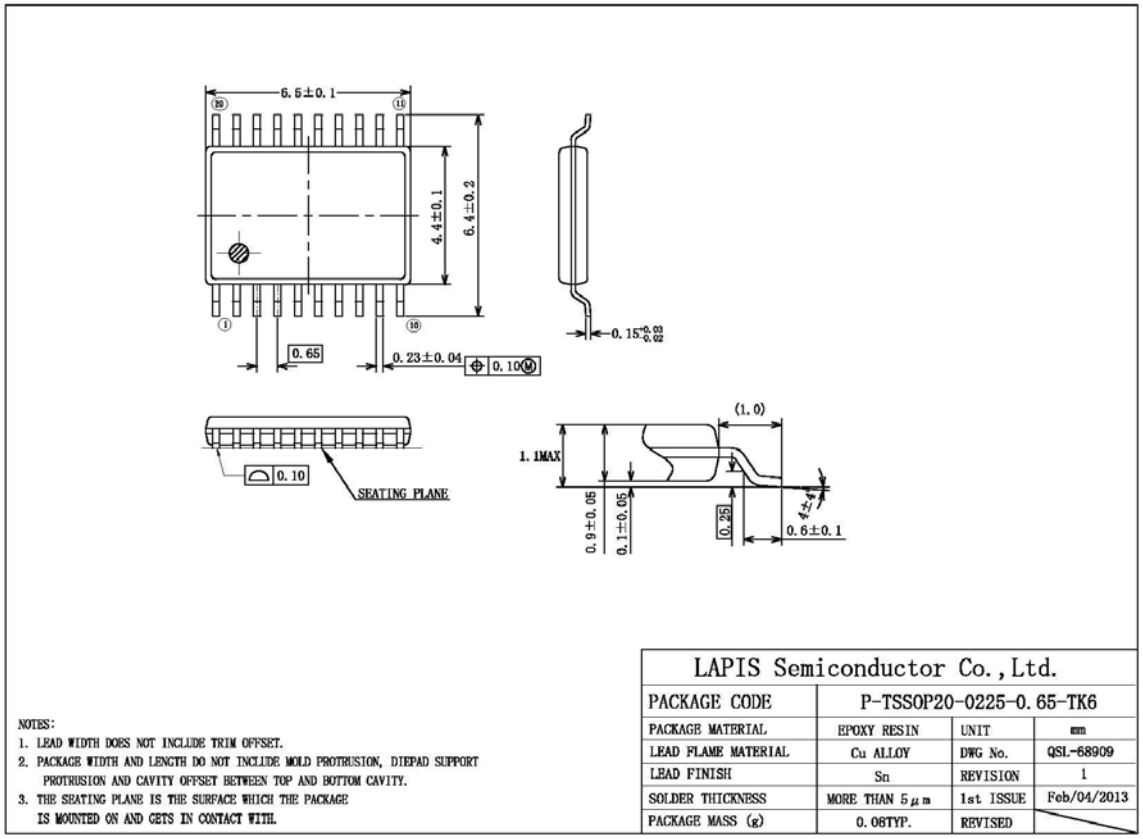
LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-SSOP16-0225-0.65-TK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68735
LEAD FINISH	Sn	REVISION	4
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Mar/26/2012
PACKAGE MASS (g)	0.069 TYP.	REVISED	Jan/30/2013

16pin WQFN



LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-WQFN16-0404-0.50-T63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68975
LEAD FINISH	Ni/Pd/Au	REVISION	1
SOLDER THICKNESS	Au/Pd Max0.15	1st ISSUE	Aug/07/2013
PACKAGE MASS (g)	0.038g	REVISED	

20pin TSSOP



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-TSSOP20-0225-0.65-TK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68909
LEAD FINISH	Sn	REVISION	1
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Feb/04/2013
PACKAGE MASS (g)	0.08TYP.	REVISED	

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL620Q130-01	Nov 12, 2015	–	–	Fromal 1st Revision

Notes

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